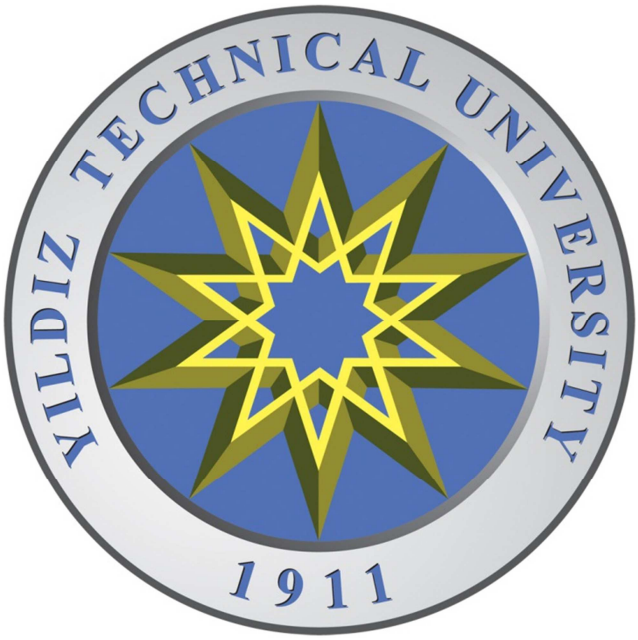


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NOVEL MULTI-TERMINAL BUILDING BLOCKS WITH TUNING ABILITY AND ITS APPLICATION IN ANALOG SIGNAL PROCESSING

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LIST OF SYMBOLS

a, b	General current transfer coefficients
A	Gain of the inverting amplifier
B	Adjuastable current gain
BW	Bandwidth
α	Non-ideal current gain
β	Non-ideal voltage gains
C	Capacitor
C_{OX}	Gate oxide capacitance per unit area
D	Frequency dependent negative resisitor
ε_i	Current tracking error
ε_v	Voltage tracking error
f	Frequency
f_0	Characteristic frequency
g_m	Transconductance of the OTA
I	Terminal current of a function block
I_O	Output current
I_B	Bias or control current of the transconductance
K, T(s)	Current or voltage transfer function
K	Transconductance parameter
L	Inductance
M_i	CMOS transistor
ϕ	Phase of all-pass filter
P, N	Input current or voltage terminals of the VDCC
Z	Auxiliary current or voltage terminals of the VDCC
X, W_N, W_P	Output current or voltage terminals of the VDCC
R	Resistance
R_p	Parasitic resistance at terminals P and W_N
μ	Free electron mobility in the channel
V	Terminal voltage of an active element
V	Terminal voltage of a function block
V_T	Thermal voltage
V_+, V_-	The voltages on non-inverting and inverting inputs of OTA
V_{DD}, V_{SS}	Supply voltages of CMOS structures
$\omega_{Z/P}$	Zero/pole frequency
W/L	CMOS transistor dimensions
φ	Phase difference between two outputs in quadrature oscillators
Y, Z	Admittance, Impedance

LIST OF ABBREVIATIONS

ABB	Analog building block
AGC	Amplitude gain control
AP	All-pass
CA	Current amplifier
CBTA	Current backward transconductance amplifier
CC	Cuurent conveyor
CCCC	Current controlled current conveyors
CCII	Second-generation current conveyor
CCII+	Positive type second-generation current conveyor
CCTA	Current conveyor transconductance amplifier
CM	Current mirror
CO	Condition of oscillation
COA	Current operational amplifier
DT	Diamond transistor
DVB	Differential voltage buffer
DVCC	Differential voltage current conveyor
DV-VB	Differential voltage voltage buffer
ECCII	Electronically controllable current conveyor of second generation
FC	Floating Capacitor
FR	Floating resistor
FDNR	Frequency dependent negative resistors
FI	Floating inductor
FO	Frequency of oscillation
FPAA	Field programmable analogue array
IC	Integrated circuit
OA	Operational amplifier
OTA	Operational transconductance amplifier
PSK	Phase shift keying
QO	Quadrature oscillator
QPSK	Quadrature phase shift keying
THD	Total harmonic distortion
VD-DIBA	Voltage differencing differential input buffered amplifier
VDTA	Voltage differencing transconductance amplifier
VLSI	Very large-scale integration

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ABSTRACT

NOVEL MULTI-TERMINAL BUILDING BLOCKS WITH TUNING ABILITY AND ITS APPLICATION IN ANALOG SIGNAL PROCESSING

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MSc. Thesis

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Based on the state-of-the-art of research in analog signal processing define a novel multi-terminal analog building block (ABB), which offers independent electronic control of its intrinsic input resistance of current inputs and/or transconductance gain and / or voltage / current transfer gains between selected terminals. This thesis is, therefore, focused on definition of other novel ABBs and, furthermore, novel filter and oscillator structure designs.

Another reason for focusing more attention on analog building blocks is given by relatively implementation of large valued elements to the integrated circuit (IC) process. For example, floating immitance simulator circuits are very useful active building blocks in many applications such as filter design, oscillator design and cancellation of parasitic elements. This is due to the fact that the use of the physical inductor and capacitor, particulary of large values, is either not permitted or is unwanted in the integrated circuit technology.

Recent work in this area indicates that immitance simulator circuits in same cases required for designing integrated circuit active filters, oscillators *etc*. Consequently, it is crucial to adapt state-of-the-art filters, oscillators for practical use, as well as illustrate the functionality for future work in this area.

Together with the immitance simulator circuits, filters, oscillators *etc.* are emphasizing stronger support for analog signal processing applications. There are implemented some special approaches to the design of multiphase oscillators. Since, fractional-order all-pass (AP) transfer section was used for the design of multiphase oscillator and

symbolical transfer function of this section contains fractional exponent α of the Laplace operator s, where fractional character is given by RC approximation of the fractional order capacitor in the structure, this feature allows synthesis of multiphase oscillators with theoretically arbitrary phase shifts between generated signals and extended range of frequency of oscillations (FO) tuning proportional to reciprocal time constant exponentiated by $1/\alpha$. Unfortunately, unavailability of simple electronic adjusting of the fractional-order capacitor limits real utilization of fractional-order-based circuits in systems for the signal generation and processing.

Summarizing, this thesis is generally aimed at the improvement, utilization or newly designed oscillators, filters *etc*. with arbitrary features. Implement the defined ABB using recent CMOS technology parameters and provide its verification in PSpice design environments. The theoretical analyses are done using SNAP software. For experimental purposes, the circuits were designed with commercially available integrated circuits using behavioral modeling approach. In order to prove the usefulness of the proposed new multi-terminal ABB, filter and oscillator design was used in several analog signal processing applications which behavior will be examined by computer simulations. The feasibility of selected circuits is also confirmed by experimental measurements.

Key words: Novel active building blocks, immitance simulator, quadrature oscillators, all-pass filters, phase shift keying, modulation

ÖZET

ÇOK-UÇLU YAPI BLOKLARININ TASARLANMASI VE ANALOG SİNYAL İŞLEMEDE UYGULANMALARI

Aslıhan KARTCI

Elektronik ve Haberleşme Mühendisliği Anabilim Dalı

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Analog sinyal işlemede son teknolojik gelişmelere dayanarak, bağımsız, mevcut giriş akımlarının iç direnciyle, geçiş iletkenliği veya seçili terminaller arasındaki voltaj ve akım transfer kazancıyla elektronik olarak ayarlanabilen çok-uçlu analog yapı blokları tanımlanmıştır. Bu nedenle, bu tezde yeni analog blok yapıları, filtre ve osilatör tasarımları üzerinde duruldu.

Analog yapı bloklarının üzerinde daha fazla durmak için bir başka neden de entegre devre üretimi sırasında büyük değerli elementlerin bu analog yapı bloklarıyla uygulanması örnek verilebilir. Örneğin, yüzen imitans simülatör devreleri filtre tasarımı, osilatör tasarımı gibi parazit unsurların iptali gibi birçok uygulamada çok yararlı aktif yapı taşlarıdır. Bu büyük değerlerli fiziksel indüktör ve kondansatör özellikle entegre devre teknolojisinde istenmeyen veya izin verilmeyen durumlara örnektir.

Bu alanda son çalışmalar entegre devre aktif filtreler, osilatörler, vb. tasarımı için gerekli olan imitans simülatör devrelerini gösterir. Sonuç olarak, pratik kullanım için filtrelerin ve osilatörlerin temel yapısının yanı sıra, bu alanda gelecekte yapılacak çalışmalar için işlevsellik göstermek için çok önemlidir.

İmitans simülatör devreleri ile birlikte filtreler, osilatörler vb. uygulamalarının analog sinyal işlemede önemli bir yeri vardır. Çok fazlı osilatör tasarımı için bazı özel yaklaşımlar uygulanmaktadır. Kesirli dereceden tüm geçiren filtereler çok fazlı osilatörde kullanılırken transfer fonksiyonunun tasarım için RC yaklaşımı ile verilen Laplace operatörü s kesirli üs a'yı içerir. Bu özellik üretilen sınyal ve $1/a$ ile genişletilen

sinyal rasında ayarlanabilir faz kaymalı çok fazlı osilatörle izin verir. Malesef ki, kesirli dereceden kapasitörlerin elektronik olarak ayarlanamamasından dolayı gerçekte üstlü dereceden devrelerin sinyal üretimi ve işlenmesini sınırlar.

Özet olarak, bu tezde genellikle varolan hatalar düzeltilerek yenisi gelistirilmiş, pratikte uygulaması yapılmış veya tamamen sıfırdan tasarlanmış yapılar üzerinde durulmuştur. Son CMOS teknolojisi parametreleri kullanılarak tanımlanan analog yapı blokları uygulanmış, PSpice programında doğruluğu kanıtlanmıştır.Gerçek ortamda test edebilmek için, davranışsal modelleme yaklaşımı kullanılarak piyasada mevcut entegre devreler ile eşdeğer bir model önerilmiş yani ticari olarak üretmi yapılan tümdevreler kullanılarak devreler tasarlanmıştır. Önerilen yeni çok-uçlu analog yapı bloklarının yararlarını ispatlamak amacıyla, çeşitli analog sinyal işleme uygulamalarıyla laboratuvar ortamında ölçümler yapılarak, tasarımı ve bilgisayar simülasyonları incelenmiştir.

Anahtar Kelimeler: Yeni aktif yapı blokları, imitans simülatörü, dördün osilatörler, tüm geçiren filtreler, faz kaydırmalı anahtarlama, modülasyon

CHAPTER 1

INTRODUCTION

1.1 Literature Review

For many reasons, it is very difficult to implement large valued inductors and floating capacitors via the integrated circuit (IC) process. Also, the floating immittance function simulators such as frequency dependent negative resistors, inductors, or capacitance multipliers are widely used in various applications instead of physically available passive elements. The two most important replacement techniques are passive element and operational simulation technique [1]. The passive element replacement technique works well if certain conditions are satisfied, but it has drawbacks at high frequencies like any other technique [2]. Thus, a number of circuits have been presented as general floating immitances [3-9] to solve this issue. A possible solution is the use of small capacitive, inductive, resistive values, to obtain higher equivalent integrated capacitance, inductance, resistance, avoiding the large silicon area.

Recently, several grounded/floating capacitance multipliers adopting either capacitance multiplication techniques, implemented using active building blocks such as several classes of second-generation current conveyors (CCIIs) [7-9], operational transconductance amplifiers (OTAs) [10], current conveyor transconductance amplifiers (CCTAs) [11], current mirrors (CMs) and current amplifiers (CAs), various active devices; current conveyor (CC) and current operational amplifier (COA), differential voltage current conveyor (DVCC) and current controlled current conveyors (CCCIIs) [12], CMOS inverters and op-amps [13], current backward transconductance amplifier (CBTA) [5], *etc.* are reported.

Several FDNR implementations using various active devices, such as positive type second-generation current conveyors (CCIIs+) [3], [14], [15], [16], voltage differencing transconductance amplifiers (VDTAs) [17], current backward transconductance

amplifier (CBTA) [5], and field programmable analogue array (FPAA) [18] were proposed in the literature.

The literature surveys show that a large number of modern circuit realizations for immitance simulators have been reported [4-17]. Unfortunately, these reported circuits suffer from one or more of following weaknesses:

- Need for passive element matching [11].
- Lack of electronic tunability, which cannot be implemented in automatic control systems.
- Excessive use of the active and/or passive elements.
- Use of floating capacitor, which is not convenient to further fabricate in IC [36], [37].
- Use of a capacity or connected to in appropriate terminal, which results in an extra pole, and consequently lower frequency of operation .

Harmonic oscillators with multiphase or/and arbitrary adjustable phase shift between output signals are still very interesting areas for many researchers, because many various active elements [19] can be beneficially utilized and allow interesting additional features in some cases. Principle of operation of known solutions can be divided to the following groups: a) lossy blocks (integrators or similar selective sections) in stepwise phase shifted cascade and full feedback (for example [20], [21], [22] and references cited therein); b) all-pass section in combination with integrators/differentiators in simple loops ([23-27] for example); c) all-pass sections (APs) in the loop ([28], [29] for example); d) other principles (see [30] for detailed discussion). Most of discussed simple solutions focus on quadrature oscillator design (for example detailed literature discussion in [31] and [32]). Some attempts to design the simple oscillators with different phase shift than 90 degrees were also provided ([30], [33] for example]). However, these solutions suffer from some drawbacks (mutually dependent oscillation condition and frequency of oscillations, required matching of several parameters and amplitudes dependent on tuning process [30]).

Unfortunately, arbitrary setting of the phase shift between output signals is not always ensured [34]. Only typical phase shifts in multiphase types of oscillators are verified (phase shifts given by $2\pi/n$, where is integer value), typically in multiples of $\pi/4$, $\pi/3$,

etc. Arbitrary phase shift means phase shift may not be in integer multiple of the minimal available phase shift generated by the basic lossy block of the structure. Moreover, solutions in [34] are quite complicated and require many active elements. However, from our point of view, it seems to be possible to generate not only integer multiples of basic phase shifts, as is presented in this contribution on a very simple example of circuit solution.

1.2 Objective of the Thesis

A circuit employing a minimum number of active and passive components is advantageous from the points of view of very large-scale integration (VLSI) implementation, area, power consumption, and cost. Also, it is well known that, in integrated circuit (IC) processes, the realization of grounded passive components, especially grounded capacitors [35], are more convenient than floating ones [36], [37]. Hence, the circuit designer should avoid using floating passive components and passive component-matching constraints as much as possible. Another point in the IC fabrication, it is impractical to realize high-valued capacitors because of occupy area. In fact, in a standard CMOS poly-silicon layers, a small-valued capacitor is equivalent, relatively to the silicon area, to thousands of transistors. This means that the integration of capacitor as large as highed-valued one is not possible. Even in some applications are necessary to have higher capacitive values.

Phase shifter or all-pass filter is one of the important circuit building block used in analog signal processing applications. Traditionally, phase shifter consists of resistors, capacitor and operational amplifier (OA). Due to the disadvantage of narrow gain bandwidth product of op-amp used and the corner frequency without provided electronically adjustable property, its applications are limited. In addition, the use of resistor, high valued capacitances in the circuit are unsuitable for IC implementation.

The main target of this thesis is the designing of the comprehensive-commercially available circuit models including their maximum adjustable parameters in relation between their terminals that may be used for the radio communications applications. Throughout this work, I particularly emphasize various interesting features of electronic controllability of the main features and also allow advanced inter-terminal features. All these features are very useful in future applications of filters, oscillators, modulators, *etc.* The model represents advanced active device and facilitates very inexpensive

verification of various theories and hypotheses without requirement of the system implementation on IC at this stage. In other words, it allows the very first but real experimental verification of the system and foregoing expensive IC fabrication.

Consequently, our approach involves deep and systematic study of electronic controllability, tuning ability, amplitude stabilization, and commercially available active devices on immitance simulators, filters, oscillators, and modulators. It is not only proposes new circuit facilities and corresponding mathematical solutions that substantially improve electronic controllability and amplitude gain control (AGC) , but also provides a deep understanding of fundamental rules in advanced analog signal processing. The joint study of immitance simulator such as floating inductors (FIs), floating capacitors (FCs), floating resistors (FRs), frequency dependent negative resistors (FDNRs) and all pass filter, control logic, and oscillator is expected to facilitate the designed phase shift keying modulation.

1.3 Thesis Outline and Main Results

This thesis consists of an introductory part comprising seven chapters and of eight main publications referred to as [P1]-[P3]. Additionally, the scope of this work is closely related to publications [38] and [39], which are summarized and seamlessly integrated into the body of the manuscript. In order to make this text accessible by a more general audience, I begin with the fundamental issues and core trade-offs related to novel ABBs. I then gradually shift toward to some integrated circuit design, simplification and applications. Finally, selected ABBs and features are considered which require specific knowledge of the state-of-art analogue sıgnal processing. Facilitating the flow of thought, the material given in the initial chapters is reused by the subsequent chapters. As such, the focus of the narration tends to transfer from more general to more detailed problem formulations and related research.

In Chapter 1, I start with the core motivation behind our research and then continue with the scope of this work by highlighting the key problems addressed in the thesis. In Chapter 2, I emphasize the importance of ABBS and provide the reader with the related background. I then discuss ABBs features in different applications, focusing more on the communication and radio systems.

In Chapter 3, the novel concept of immitance simulator and phase-shift keying is mentioned and recent progress in design procedure is summarized including our own

contributions. Our results confirm that the proposed solutions are successful in bridging across the indicated system vulnerabilities. Chapter 6 concludes the introductory part and outlines some interesting directions for future work. Finally, Chapter 4 summarizes the publications constituting the second part of this thesis and highlights the author's contribution to them.

CHAPTER 2

NOVEL ACTIVE BUILDING BLOCKS AND THEIR PROPERTIES

2.1 History

Analog circuits act as a bridge between the real world and digital systems, which are fundamentally necessary in many of today's complex, high performance systems and have naturally, occurred signals. Although, operational amplifiers were the un-avoided building blocks for analog circuit design at the beginning, their limited performance such as bandwidth, slew-rate *etc.* leads the analog designer to search other possibilities and other building blocks. As a result, a huge number of active elements for current-, voltage-, and mixed-mode were introduced for analogue signal processing [19].

Experimental verification via their on-chip fabrication is expensive and time-consuming. It turns out that the development of the applications of the active elements can be effective enough in the following steps: 1) The implementation of a novel circuit element from commercial integrated circuits (ICs). 2) The manufacturing of a concrete application circuit. 3) The measurements and verification. 4) The chip design and manufacturing based on the knowledge acquired in the above steps. Option 1 to 3 are performed in the belief that if the specimen built from discrete elements works well, then it's appropriate IC version, designed by a professional designer and fabricated via up-to-date IC technology, will work even better.

In respect of the difficulty of practical implementation of the active elements, simplified version is described. In this chapter, I introduce and developed different active elements with their commercially available equivalent. These active building blocks (ABBs) are further used in this thesis for various filter and oscillator designs.

2.2 Voltage Differencing Current Conveyor - VDCC

2.2.1 Literature Background

Recently, various active building blocks have been introduced in [19], where voltage differencing current conveyor (VDCC) is one of them. Since VDCC provides electronically tunable transconductance gain in addition to transferring both current and voltage in its relevant terminals, it is very suitable for the design of functional generators [40], inductor simulators [41], [42], triple-input single-output filter with independently adjustable filter parameters [43], reconfigurable reconnection-less first-order voltage-mode multifunctional filter [44], and single resistance controlled sinusoidal oscillator [45].

2.2.2 Description and Properties

The block diagram of a VDCC ideally characterized by equations $I_Z = g_m(V_P - V_N)$, $V_X = V_Z$, $I_{W_P} = I_X$, and $I_{W_N} = -I_X$ is demonstrated in Figure 2.1, where P and N are input terminals; Z auxiliary terminal; X, W_P and W_N are output terminals. Except the X terminal, all of the terminals exhibit high impedance. This conception was used in [19], [46]. The first part of the VDCC is realized as operational transconductance amplifier (OTA) to convert the input voltage to current from the difference between (V_P - V_N) with transconducance gain (g_m). Second part is CCII, which carries out the X terminal current to W_N and W_P [15].

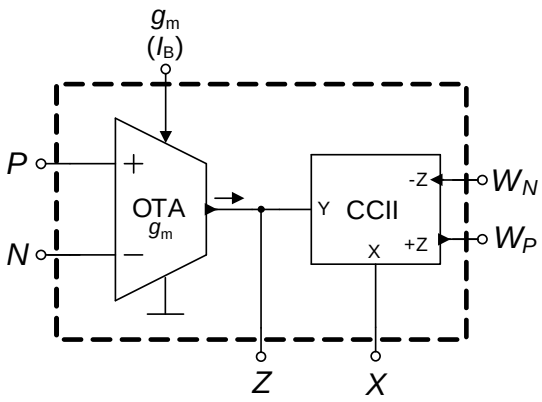


Figure 2.1 The block diagram of VDCC

The CMOS implementation of the VDCC is given in Figure 2.2, in which the transconductance section is realized by using the transistor M21 - M28, which is formed by MOS coupled pair and current mirrors. Bias current reference (for differential.pair between M1 - M4 at X, Z terminals) can be used also for biasing of the OTA section (between M21 - M24 at N, P terminals) but without any further control of g_m. We will assume that all MOS devices operate in the saturation region. Then the output current I_o can be given by:

$$I_o = g_m V_{in} = \left(\sqrt{2 I_B K}\right) V_{in}, \tag{2.1}$$

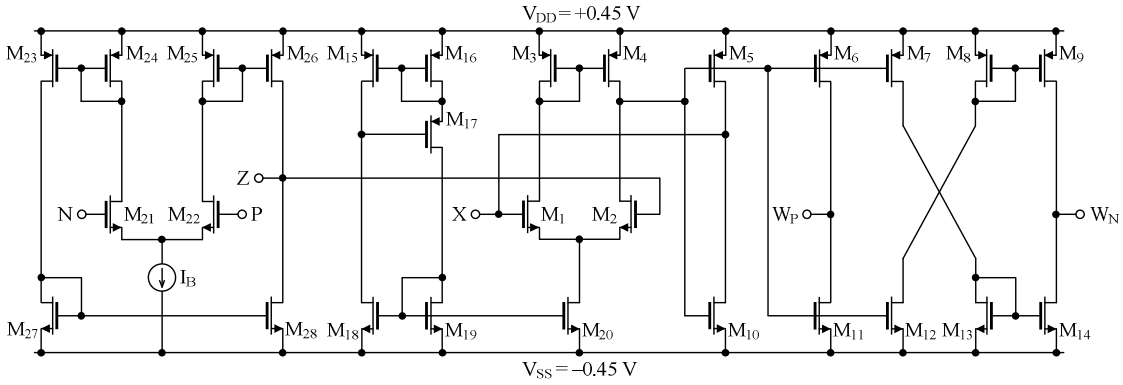


Figure 2.2 VDCC CMOS implementation

where V_{in} is the differential input voltage ($V_{in} = V_p - V_n$), I_B is the bias current, $K = \mu C_{ox} W/2L$ is the transconductance parameter, μ is the mobility of the carrier, C_{ox} is the gate-oxide capacitance per unit area, W is the effective channel width, L is the effective channel length. The dimensions of the MOS transistors used in the VDCC implementation are given in Table 2.1.

Table 2.1 Aspect ratios of transistors in VDCC.

PMOS Transistors	W (µm) / L (µm)	NMOS Transistors	W (µm) / L (µm)
M3, M4	14.4 / 0.36	M1, M2	7.2 / 0.36
M5 – M9	28.8 / 0.36	M10 – M14	6.66 / 0.36
M15	0.36 / 0.09	M18, M19	0.72 / 0.09
M16, M17	1.8 / 0.09	M20	3.24 / 0.09
M23 – M26	5.76 / 0.18	M21, M22, M27, M28	2.88 / 0.18

In the design transistors were modeled by the Predictive Technology Model (PTM) 90 nm level-7 CMOS process BSIM3v3 parameters (V_{TN0} = 0.2607 V, μ_N = 0.017999999 cm^2/(Vs), V_{TP0} = –0.303 V, μ_P = 0.0055 cm^2/(V·s), T_{OX} = 2.5 nm) [13]. During simulations the biasing current I_B was chosen as 63 µA, which results g_m equal to 501.5 µS.

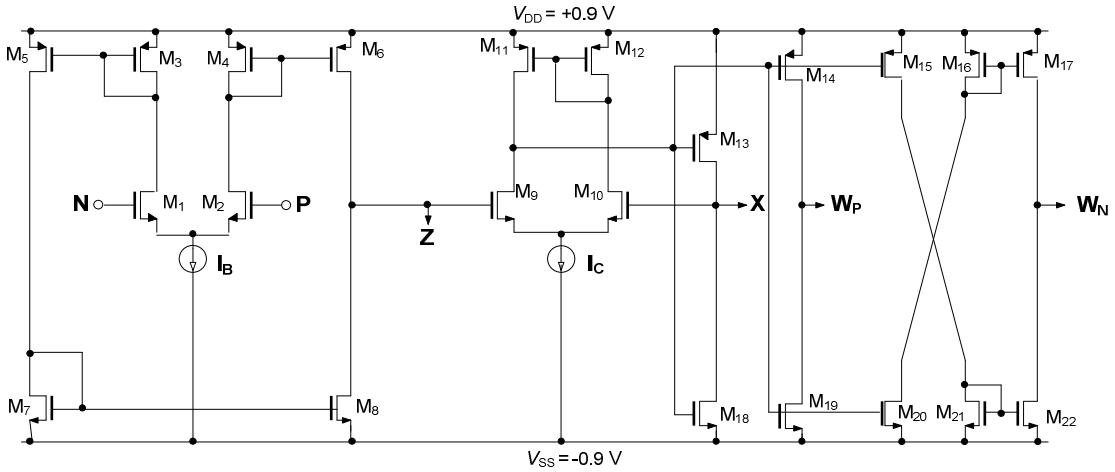


Figure 2.3 VDCC CMOS implementation [46]

The CMOS implementation of the VDCC is given in Figure 2.3. The aspect ratios of the transistors are given in Table 2.2. The MOS transistors are simulated using TSMC CMOS 0.18 µm process model parameters [47]. The supply voltages, are selected as $V_{DD} = -V_{SS}$= 0.9 V. The power consumption of the proposed VDCC is approximately 0.869 mW.

Table 2.2 Aspect ratios of transistors in VDCC [46]

Transistörler	W/L (µm)	Transistörler	W/L (µm)
M1-M4	3.6/1.8	M11-M12	9/0.72
M5-M6	7.2/1.8	M13	14.4/0.72
M7-M8	2.4/1.8	M14-M17	14.4/0.72
M9-M10	3.06/0.72	M18-M22	0.72/0.72

A detail should be noted about necessity of this implementation as bias control for R_X while Figure 2.2 allows similar features. The current which is from the inverters M13 and M18 or M14 and M19 through B - class amplifier, is not defined therefore in some case it may consume really high power consumption. Another disadvantage is this configuration can not be used in practice by microelectronics designers even it works well.

2.2.3 Terminal Parasitics Analysis

For a complete analysis, it is important to take into account parasitics of active element shown in Figure 2.4: $I_Z = g_m(V_P - V_N)$, $V_X = \beta V_Z$, $I_{W_P} = \alpha_1 I_X$, $I_{W_N} = -\alpha_2 I_X$, where α_j represents current gain and β represents voltage gain of the VDCC that differ from their ideal values by tracking errors ε_{ij} and ε_v ($|\varepsilon_{ij}|$, $|\varepsilon_v| << 1$), where j = 1, where j = 1, 2.

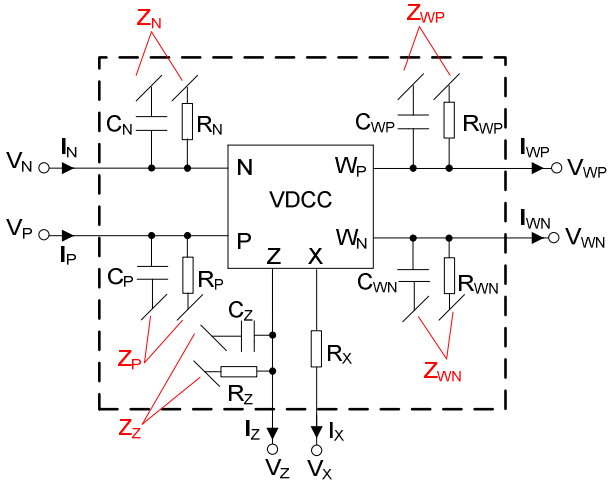


Figure 2.4 The model of the VDCC including parasitics

- The parasitic resistances R_N, R_P and parasitic capacitances C_N, C_P appear between the high-impedance N and P input terminals of the VDCC and ground, respectively.

- The parasitic resistance R_Z and parasitic capacitance C_Z appear between high-impedance Z auxiliary terminal of the VDCC and ground, respectively.

- The parasitic resistance R_X appears at the low-impedance terminal X of the VDCC.

- The parasitic resistances and capacitances R_{W_P}, R_{W_N}, and C_{W_P}, C_{W_N} appear between the high - impedance W_P and W_N output terminals of the VDCC and ground, respectively.

- The high-impedances on emitter and base input terminals of the OPA660 appear the typical values 1 MΩ // 2.1 pF and 455 kΩ // 2.1 pF, respectively.

- The high-impedance on common terminal of the OPA660 appears the typical values 25 kΩ // 4.2 pF.

2.3 A Commercially Available Operational Transconductance Amplifier - OPA660

2.3.1 Literature Summary

The operational transconductance amplifier (OTA) is an amplifier whose differential input voltage generates an output current and published by the authors in [48] as the general public the new CMOS OTA architectures and new filter realizations. Thus, the ideal OTA is a voltage-controlled current source (VCCS) with the possibility of electronic adjustment of transconductance g_m. The first commercially available integrated circuit units were produced by RCA in 1969. A commercially available OTA element is the circuit OPA660 (Texas Instruments) which has three terminals - a high-impedance input (base), a low impedance input/output (emitter), and the current output (collector) [49]. Due to its unique performance features, it is suitable for a wide variety of applications such as AGC amplifiers, LED driver circuits for Fiber Optic Transmission, integrators for fast pulses, fast control loop amplifiers, and control amplifiers for capacitive sensors and active filters applications.

2.3.2 Description and Properties

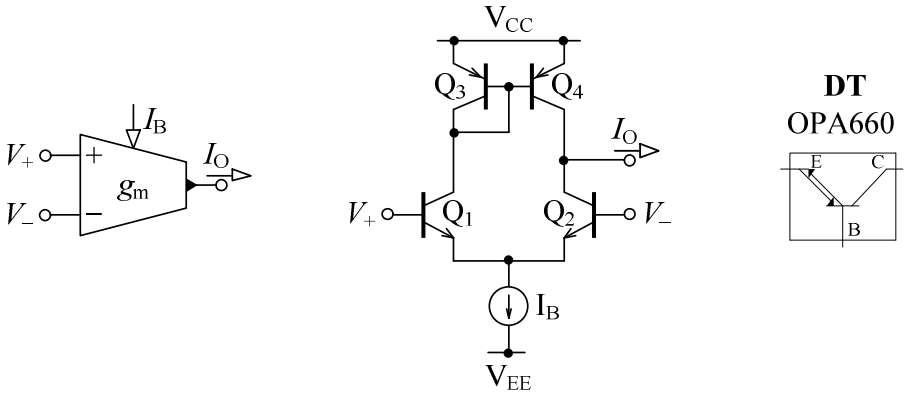
The schematic symbol and simple bipolar implementation of OTA are shown in Figure 2.5 (a) and Figure 2.5 (b). In Figure 2.5 (b), transistors Q_1 and Q_2 operate as a differential amplifier to convert an input voltage to an output current and transistors Q_3 and Q_4 work as a simple current mirror when I_B is an input bias current. The output current of the OTA is given by the following equation:

$$I_o = g_m(V_+ - V_-), \tag{2.2}$$

where V_+ and V_- are the voltages on non-inverting and inverting inputs of OTA with respect to the ground. The ideal OTA amplifier is characterized by a finite, frequency-independent transconductance gm while its input and output impedances are theoretically infinite. For a bipolar OTA in Figure 2.5 (b), the transconductance can be expressed as:

$$g_m = \frac{I_B}{2V_T}, \tag{2.3}$$

where the V_T is the thermal voltage (approximately 26 mV at 27 C) and the I_B is the control current adjusting the transconductance g_m of the OTA.



(a) (b) (c)

Figure 2.5 (a) Schematic symbol (b) and bipolar implementation of OTA (c) Schematic symbol of OPA660

The commercially active element OPA660 consists two sections. The buffer section of the OPA660 is an open-loop buffer consisting of complementary emitter-followers. The OPA660 symbol in Figure 2.5 (c) for the OTA section is similar to a transistor. Applications circuits for the OTA look and operate much like transistor circuits - the transistor, too, is a voltage-controlled current source. The three terminals of the OTA are B, E, and C. The OTA offers many advantages over a discrete transistor. The OTA is self-biased, simplifying the design process and reducing component count. The OTA is far more linear than a transistor. Transconductance of the OTA is constant over a wide range of collector currents - this implies a fundamental improvement of linearity [49].

2.4 A Commercially Available Current Mode Multipliers - EL2082 and EL4083

2.4.1 Literature Summary and Introduction

Analog multipliers are composed of the essential circuit elements of analog signal processing systems. They include a modulator, frequency doubler, rectifier, variable gain amplifier, *etc*. The multiplier is used not only as computation building block but also as a programming element in systems such as filters, neural networks, mixers, and modulators in communication systems. Several MOS four quadrant multipliers have been reported but all can be categorized into two groups based on its MOS operating region, linear and saturation. The operation of the multiplier only in linear or saturation region limits the input-voltage range, so the multiplier has wider input-voltage range as a result of operation in linear and saturation regions complementally. The analog circuit design using the current-mode approach has several advantages as wide bandwidth, high slow rate, low power consumption, and simple circuitry [50].

2.4.2 EL2082

The general purpose variable gain control building block, EL2082 is a two-quadrant multiplier, so that zero or negative control voltages do not allow signal feed through and very high attenuation is possible. The EL2082 works in current mode rather than voltage mode, so that the input impedance is low and the output impedance is high. Though, it represents electronically controllable second-generation current conveyor (ECCII-) type. This allows very wide bandwidth for both large and small signals. It operates also as adjustable current amplifier (*B*) because of consisting voltage controllable current gain [51]. According to [51], the gain error of the current multiplier EL2082 for $V_G = 2V$ is about -3.8 %. In the case of the proposed bipolar implementation, the gain error can be affected by using not precisely matched bipolar transistors.

2.4.3 EL4083

The EL4083 is a current mode four quadrant multiplier. It produce a patent pending current in, current out four quadrant multiplier. Input and output signal summing and direct interface to other current mode devices can be accomplished by simple connection to reduce component count and preserve bandwidth. The bias current is

programmable to accommodate the voltage and power dissipation constraints of the package and available systems supplies. It features high speed (both inputs), low distortion, low noise, wide supply conditions, and 0.2dB gain tolerance to 25MHz [52].

2.5 A Commercially Available Amplifiers - TL072, AD830, and VCA610

2.5.1 Literature Summary and Description

An amplifier is an electronic device that increases the power of a signal. It works as taking energy from a power supply and controlling the output to match the input signal shape with larger amplitude. In this way, an amplifier modulates the output of the power supply so the output signal gets stronger than the input signal. An amplifier is effectively the opposite of an attenuator while an amplifier provides gain, an attenuator provides loss.

The four basic types of electronic amplifiers are voltage amplifiers, current amplifiers, transconductance amplifiers, and transresistance amplifiers. A further distinction is whether the output is a linear or nonlinear representation of the input. Amplifiers can also be categorized by their physical placement in the signal chain.

2.5.2 TL072

The TL072 JFET-input operational amplifier is designed to offer a wider selection than any previously developed operational amplifier. The device features high slew rates, low-input bias and offset currents, and low offset-voltage temperature coefficient. The low harmonic distortion and low noise make the TL072 ideally suited for high-fidelity and audio preamplifier applications. A typical application for an operational amplifier is an inverting amplifier. This amplifier takes a positive voltage on the input, and makes it a negative voltage of the same magnitude. In the same manner, it also makes negative voltages positive [53]. Note that it has quite low GBW, so it is better to use OPA2650 or LT1364 for high GBW with tens and hundreds of MHz.

2.5.3 AD830

The AD830 is configured to produce the difference of the signals, in which the applied differential signal is exactly reproduced at the output relative to a separate output common. The key feature of this topology is the use of two, identical voltage-to-current converters, g_m, that make up input and feedback signal interfaces. In other words, two

g_m stages, summing high impedance node and buffer; so 4 inputs (two differential) are available. It can fork as VDDA with feedback.

2.5.4 VCA610

The VCA610 is a wideband, continuously variable, voltage-controlled gain amplifier. It provides linear-dB gain control with high impedance inputs. It is designed to be used as a flexible gain-control element in a variety of electronic systems. The circuit's basic voltage amplifier responds to the control of an internal gain-control amplifier. At its input, the voltage amplifier presents the high impedance of a differential stage, permitting flexible input impedance matching.

2.6 A Commercially Available Quad Differential Comparators - LM239

There are several types of LMx29x as LM129, 229, 339. The functionality is same but temperature range, *etc.* is different. They are used widely in military and standard utilization.

2.6.1 Description and Properties

The LM239 is a dual comparator with the ability to operate up to 36 V on the supply pin. This standard device has proven ubiquity and versatility across a wide range of applications. This is due to very wide supply voltages range (2 V to 36 V), low I_q, and fast response of the device. This device is Q100 qualified and can operate over a wide temperature range (–40°C to 125°C). The open-drain output allows the user to configure the output logic low voltage (VOL) and allows the comparator to be used in AND functionality.

LM239 consists of a PNP Darlington pair input, allowing the device to operate with very high gain and fast response with minimal input bias current. The input Darlington pair creates a limit on the input common-mode voltage capability, allowing LM239 to accurately function from ground to (VCC – 1.5 V) differential input. This is enables much head room for modern day supplies of 3.3 V and 5 V. The output consists of an open-drain NPN (pull-down or low-side) transistor. The output NPN sinks current when the positive input voltage is higher than the negative input voltage and the offset voltage.

CHAPTER 3

ACTIVE BUILDING BLOCKS IMPLEMENTATIONS AND DESIGN CONSIDERATIONS

3.1 Introduction and Motivation

Due to disadvantages of conventional inductors, active element-based passive element design is very desirable to designers today. During the last few decades, various grounded element simulators have been created using different high-performance active building blocks. However, they employ excessive number of active and passive components. Thus, the aim is to create general immitance simulator using less-number of element in compact form and their applications.

Another part of this section attempts on quadrature oscillators and first-order all pass filters. Quadrature oscillators operating at RF bands and generating unchangeable output signals are mainly determined for applications in modern digital multi-state modulations and demodulations (quadrature phase shift keying - QPSK for example) as source of carrier signal (coherent cosine and sine wave components) in many communication systems. All pass filter that the famous phase shifter is usually provided in first order form due to the simple circuit configuration and the characteristic of all-pass filter same as phase shifter provides constant gain for magnitude and frequency-dependent phase response. Because of all this specification, we use these structures in phase shift keying modulation.

Summarizing, main part of the thesis will concentrate on application possibilities of the defined functional blocks. In the first step the theoretical analyses are done using SNAP software [54]. To verify the behavior of the proposed circuits, defined active elements are implemented using bipolar or CMOS internal structures. The feasibility of selected circuits is also confirmed by experimental measurements.

3.1.1 General Background

A large number of circuit topologies have been proposed in the literature for analog signal processing such as active filters, oscillators, immittance simulators *etc.*[3-33] . At the beginning, approximately until twenty years ago, the researchers were proposing this type circuit topologies without giving any realization circuit and application example or another important missing main factor was the influence of the limitations caused by the realization topologies and employed active elements such as bandwidth, slew-rate, input and output impedances *etc.* Therefore, the main problem was how to realize these topologies and how to apply them to practical work.

Nowadays, it is possible today to realize simply these type of topologies for analog signal processing, with the advances in modern technologies such as CMOS, BiCMOS *etc.* Furthermore, realization of the proposed circuit, circuit performance limitations, these circuits applications type in practical world, the desired output signal pick-up way also demonstrate now the new trend in analog circuit design. The application area is from very low frequencies at several Hz levels of biomedical signals to RF applications operating at GHz level, from EEG signals to cognitive radio and encrypted communications or low-noise amplifiers in wireless communications. Therefore the designer should know the limitations that influence the performance of his circuit before realization phase.

3.2 General Element Simulator

Analog integrated circuits often require high-valued Physical inductors, capacitors, particularly of large values, characterized by high accuracy and linearity that occupy small silicon area. Although this is difficult to achieve, given the fact that two polysilicon layers available in modern fabrication processes typically result in relatively small element values. This was the motivation for the designers to develop a wide diversity of architectures including active devices for general element simulators. Some schemes offer a very high multiplication factor, although they have poor accuracy. Others offer very high accuracy at the expense of increased silicon area and power consumption.

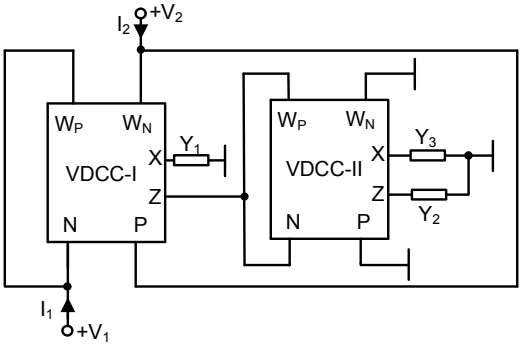


Figure 3.1 General floating element simulator circuit

Considering floating element simulator circuit in Figure 3.1 and assuming $\alpha_{12} \approx \alpha_{11} = \alpha_1$, the short circuit admittance matrix of this circuit can be written as:

$$y_{ij} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} = \frac{\alpha_1 \beta_1}{\beta_2 \alpha_2} \frac{Y_1 Y_2 g_{m1}}{Y_3 g_{m2}} \begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix}, \tag{3.1}$$

where $\alpha_{12} \approx \alpha_{11} = \alpha_1$, $\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = y_{ij} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$. Note that by setting either $+V_1 = 0$ or $+V_2 = 0$, the defined general element simulator can also be used as a grounded ones.

The circuit in Figure 3.1 can be easily modified to realize nth -times floating element simulator circuit, as it is shown in Figure 3.2. If the n is equal to odd; floating inductor (FI) and floating capacitor (FC) definitions changed each other, others stay same. Contrary, if the n is even number; all definitions and equations are valid as mentioned above.

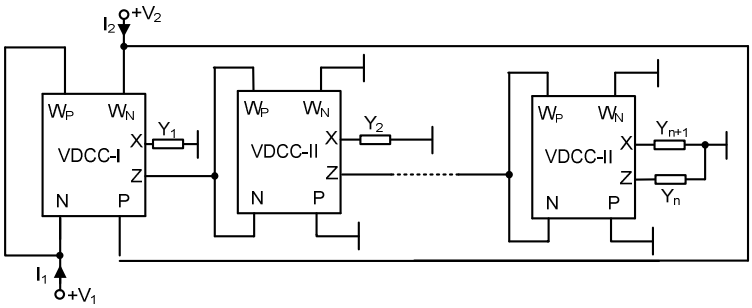


Figure 3.2 *n*th - times floating element simulator circuit

If $Y_1 = sC_1$, $Y_2 = sC_2$, $Y_n = sC_n$ and $Y_{n+1} = G_{n+1}$ are chosen for the circuit depicted in Figure 3.2, the short circuit admittance matrix of the floating *n*th-order frequency dependent element is found to be:

$$[Y_D^n] = \frac{\alpha_1\alpha_2...\alpha_{n-1}\beta_1\beta_2...\beta_{n-1}}{\alpha_n\beta_n} \frac{s^n g_{m1}g_{m2}...g_{m(n-1)}C_1C_2...C_n}{g_{mn}G_{n+1}} \begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix}. \quad (3.2)$$

Terminal Parasitics Analysis:

Considering the parasitics of the VDCC shown in Figure 2.4, the non-ideal general simulator circuit shown in Figure 3.3 can be characterized as follows:

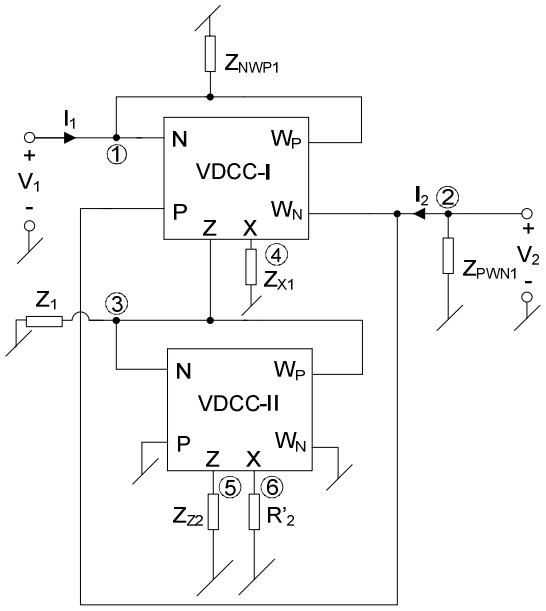


Figure 3.3 Proposed general floating element circuit including parasitics

- At the node 1 and 2, the parasitic terminals of VDCC-I, N, W_P and P, W_N are parallel respectively, and in analysis they are shown as $Z_{NW_p1} = Z_{N1} // Z_{W_p1}$ and $Z_{PW_N1} = Z_{P1} // Z_{W_N1}$.
- At the node 3, the parasitic terminal Z of VDCC-I, and the parasitic terminals of VDCC-II, N, W_P are paralel each other, described as $Z_1 = Z_{Z1} // Z_{N2} // Z_{W_p2}$.
- At the node 4, the parasitic terminal X of VDCC-I appears low resistance and this resistance is series with this terminal capacitance, described as $Z_{X1} = R_{X1} + 1/sC_1$. It means that R_X is always in series with C_1 or another external passive element.
- At the node 5, the parasitic terminal Z of VDCC-II appears high resistance and this resistance is parallel with terminal capacitance, described as $C'_{Z2} = C_2 + C_{Z2}$ while $Z_{Z2} = R_{Z2} // sC'_{Z2}$.

- At the node 6, the parasitic terminal X of VDCC-II appears low resistance and this resistance is series with parasitic resistance, described as $R'_2 = R_{X2} + R_2$.

Considering these non-idealities for the circuit shown in Figure 3.1, the input-output currents and voltages relationship is given by:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = X \begin{bmatrix} \alpha_{11} + \dfrac{Z_{X1}}{g_{m1} Z_{PW_N 1} Z \alpha_{11} \beta_1} & -\alpha_{12} \\ \alpha_{11} & \dfrac{Z_{X1}}{g_{m1} Z_{NW_P 1} Z \alpha_{12} \beta_1} - \alpha_{12} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}, \tag{3.3}$$

where $X = \dfrac{g_{m1} Z \beta_1 Z_{NW_P 1} Z_{PW_N 1}}{g_{m1} Z \beta_1 (Z_{PW_N 1} \alpha_{11} - Z_{NW_P 1} \alpha_{12}) + Z_{X1}}$, and $Z = \dfrac{R_2 Z_1}{-g_{m2} Z_{Z2} Z_1 B_2 A_{22} + R_2}$.

From equations (3.1) it can be seen that depending on the choice of passive components a floating FDNR, FI, FC, and FR simulators can be realized as given below. Moreover, by grounding one of its terminals, it can also be used for grounded simulators.

3.2.1 Frequency Dependent Negative Resistor

The first frequency dependen t negative resistor (FDNR) element was introduced by Bruton in 1969 [55] and it was designed using operational amplifiers. However, due to smaller dynamic range, narrow bandwidth, and higher power consumption of operational amplifiers, the active building block (ABB) design received considerable attention during the last decade and FDNRs are very useful for designing and synthesis of active filters and they can be used in floating-grounded inductance applications [56].

According to equation (3.1); if $Y_1 = sC_1$, $Y_2 = sC_2$ and $Y_3 = G_3$ are selected, a floating FDNR is implemented as follows:

$$[Y_D] = \frac{\alpha_1 \beta_1}{\alpha_2 \beta_2} \frac{s^2 C_1 C_2 g_{m1}}{G_3 g_{m2}} \begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix}, \tag{3.4}$$

which represents a floating FDNR whose parameter is given by $D_f = \dfrac{\alpha_1 \beta_1}{\alpha_2 \beta_2} \dfrac{C_1 C_2 g_{m1}}{G_3 g_{m2}}$. In ideal conditions, $D_{f-ideal} = \dfrac{C_1 C_2 g_{m1}}{G_3 g_{m2}}$. Hence, the proposed circuit of Figure 3.1 behaves as an ideal floating FDNR.

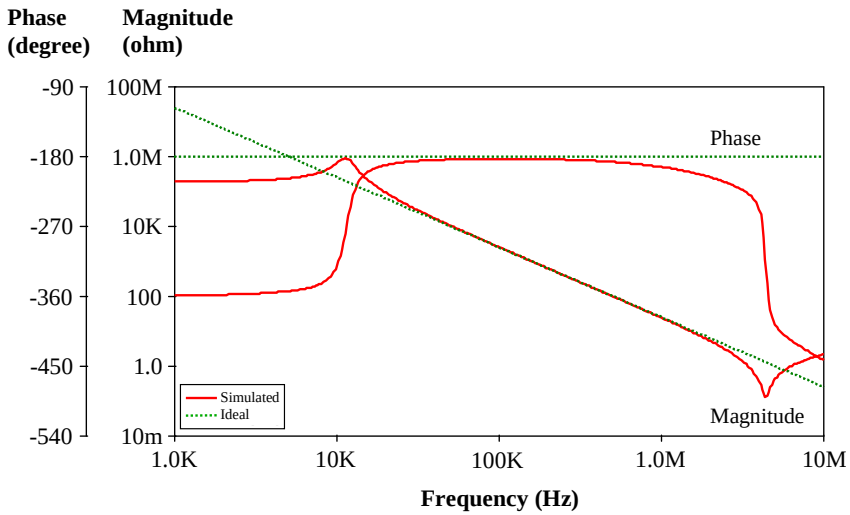


Figure 3.4 Impedance responses of the FDNR simulator vs. frequency

To verify the theoretical analysis, the behavior of the floating inductance simulator from Figure 3.1 has been verified by SPICE simulations using CMOS implementation of VDCC given in Figure 2.2. During simulations the biasing currents $I_{B1} = I_{B2}$ were chosen as 63 µA, which results $g_{m1} = g_{m2}$ equal to 501.5 µS. The passive element values have been chosen as follows: $C_1 = C_2 = 1$ nF and $R_3 = 1$ kΩ to obtain $D = 1$ fFs. Ideal and simulated magnitude and phase responses of the impedance of the proposed FDNR are shown in Figure 3.4. The proposed FDNR total power dissipation is 556 µW and transistors occupy total area of 134.46 μm^2. Considering 10 degree difference in phase, the working frequency of the FDNR is from 20.8 kHz to 747.4 kHz.

3.2.2 Capacitance Multiplier

The implementation of high-valued capacitors in integrated silicon circuits is limited by the occupy chip area. Due to this limitation, there are some options: use and pay for external capacitors, use and pay for expensive new process features or reduce the needed capacitors. When none of these three solutions is adequate, we have to look for other options. One of them is to implement an active circuit that emulates a capacitance several times larger than that of the physical capacitor.

In this chapter, I propose two floating / grounded capacitance multiplier employing two VDCC, one grounded resistor, one grounded capacitor and one VDCC, one grounded resistor, and one grounded capacitor. Both of the proposed topologies ideally provide lossless capacitor.

The first proposed circuit for realizing a floating lossless electronically-controllable C-Multiplier depicted in Figure 3.1, is designed while $Y_1 = G_1$, $Y_2 = sC_2$, and $Y_3 = G_3$. The short circuit admittance matrix of the FC is found to be from equation (3.1):

$$[Y_C] = \frac{\alpha_1\beta_1}{\alpha_2\beta_2}\frac{sC_2G_1g_{m1}}{G_3g_{m2}}\begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix}, \tag{3.5}$$

where $C_f = \frac{\alpha_1\beta_1}{\alpha_2\beta_2}\frac{C_2G_1g_{m1}}{G_3g_{m2}}$. In ideal conditions, $C_{f-ideal} = \frac{C_2G_1g_{m1}}{G_3g_{m2}}$.

The value of grounded capacitor C_2 can be multiplied by a constant which can be tuned electronically by using transconductance values of the VDCCs or can be controlled through grounded resistors.

The proposed circuit shown in Figure 3.1 is simulated with the following passive element values and using CMOS implementation of VDCC given in Figure 2.2: $R_1 = 1/G_1 = 1\ \text{k}\Omega$, $R_3 = 1/G_3 = 100\ \text{k}\Omega$, $C_2 = 100\ \text{pF}$ to obtain the $C_f = 0.125\mu\text{F}$ in grounded form as solved below:

$$C_{f-ideal} = \frac{C_2G_1g_{m1}}{G_3g_{m2}} = \frac{(100\ \text{pF})(100\ \text{k}\Omega)(22\ \mu\text{S})}{(1\ \text{k}\Omega)(277\ \mu\text{S})} = 0.125\ \mu\text{F}. \tag{3.6}$$

Transconductances (g_{m1} and g_{m2}) and bias currents are calculated for VDCC-I $I_{B1} = 50\ \mu\text{A}$ while $g_{m1} = 22\ \mu\text{S}$. And for VDCC-II $I_{B2} = 1\ \mu\text{A}$ while $g_{m2} = 277\ \mu\text{S}$ ($I_{C1} = I_{C2} = 100\ \mu\text{A}$)

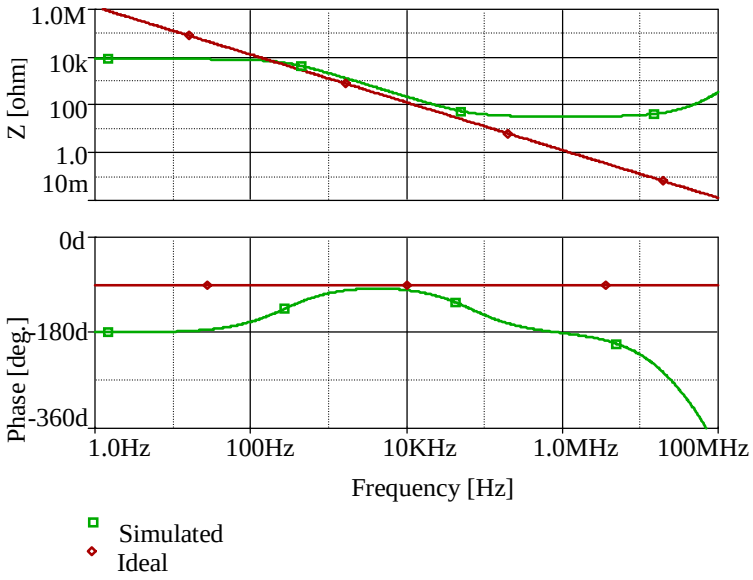


Figure 3.5 Ideal and simulated capacitance multiplier phase and magnitude (empedans) response

The ideal and simulated C-Multiplier empedans-phase charachteristic is shown as Figure 3.5 to specify maximum band-range. It can be seen that the simulated and ideal responses are very close to each other in the frequency range of 100 Hz to 50 kHz. According to non-ideal analysis, the input terminal parasitic empedans is caused by low frequency deviation, Z_1 parasitic empedans is caused by high frequency deviation. The high frequency range is required sensitive VDCC design. Additionally, the time domein analysis is shown in Figure 3.6 when 10 kHz sinus signal and 10 mV amplitude are applied. From figures it can be seen that the theoretical and simulated results are in good agreement.

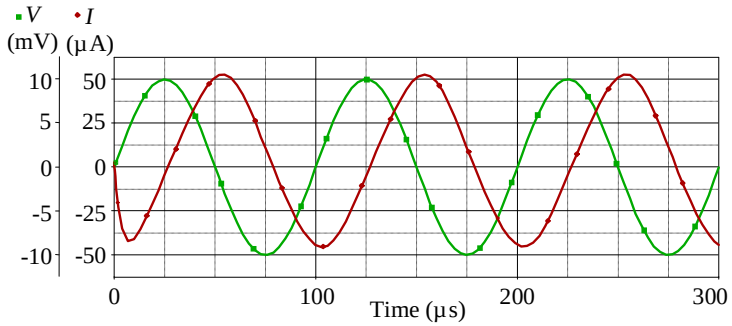


Figure 3.6 Waveforms of voltage and current for the floating capacitance multiplier

The second circuit for realizing a floating lossless electronically-controllable C-Multiplier is shown in Figure 3.7. The circuit is constructed with single VDCC, one grounded resistor, one grounded capacitor, and its short circuit impedance matrix can be written as:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = sC_{eq} \begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}, \tag{3.6}$$

from which:

$$C_{eq} = CRg_{\mathrm{m}}. \tag{3.7}$$

From equations (3.6) and (3.7) it can be seen that the equivalent capacitance value is controllable electronically and linearly with transconductance gain of VDCC.

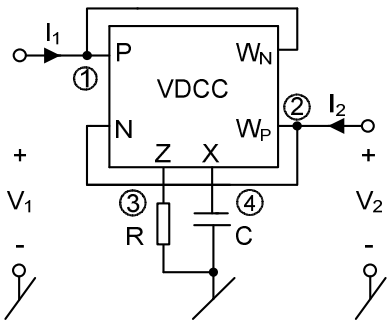


Figure 3.7 Proposed C-Multiplier circuit

Terminal Parasitics Analysis:

For a complete analysis, it is important to take into account parasitics of active element shown in Figure 2.4: $I_Z = g_m(V_P - V_N)$, $V_X = \beta V_Z$, $I_{W_P} = \alpha_1 I_X$, $I_{W_N} = -\alpha_2 I_X$, where α_j represents current gain and β represents voltage gain of the VDCC that differ from their ideal values by tracking errors ε_{ij} ve ε_v ($|\varepsilon_{ij}|$, $|\varepsilon_v| << 1$), where j = 1, 2.

- The parasitic resistances R_N, R_P and parasitic capacitances C_N, C_P appear between the high-impedance N (1 MΩ // 2.1 pF) and P (455 kΩ // 2.1 pF) input terminals of the VDCC and ground, respectively.

- The parasitic resistance R_Z, and parasitic capacitance C_Z appear between high-impedance Z auxiliary terminal of the VDCC and ground, respectively and their typical values are 25 kΩ // 4.2 pF.

- The parasitic resistance R_X appears at the low-impedance terminal X of the VDCC and its typical value is 95 Ω.

- The parasitic resistances and capacitances, R_{W_P}, R_{W_N}, and C_{W_P}, C_{W_N} appear between the high-impedance W_P and W_N output terminals of the VDCC and ground, respectively and their typical values are 1 MΩ // 5 pF.

Considering the effect of aforementioned non-idealities on the proposed circuit implemented as shown in Figure 3.8, the following useful analysis can be provided:

- At the node 1 and 2, the parasitic terminals of VDCC, P, W_N and N, W_P are parallel respectively, and in analysis they are shown as $Z_{PW_N} = Z_P // Z_{W_N}$ and $Z_{NW_P} = Z_N // Z_{W_P}$.

- At the node 3, the parasitic terminal Z of VDCC appears high resistance and this resistance is parallel with parasitic capacitance, described as $Z_Z = R'_1 // sC_Z$, while $R'_1 = R_Z // R$.

- At the node 4, the parasitic terminal X of VDCC appears low resistance and this resistance is series with this terminal capacitance, described as $Z_X = R_X + 1/sC$.

Hence, the short circuit impedance matrix in Equation (3.8) turns to:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \frac{\beta g_m Y_X}{Y_Z} \begin{bmatrix} \frac{Y_{PW_N} Y_Z}{\beta g_m Y_X} + \alpha_2 & -\alpha_1 \\ -\alpha_2 & \frac{Y_{NW_P} Y_Z}{\beta g_m Y_X} + \alpha_1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}. \tag{3.8}$$

The parasitic zero of the impedance at high frequencies can be seen in Figure 3.9 as:

$$f_o = 1/2\pi C R_X, \tag{3.9}$$

and the frequency dependent AC model of C-Multiplier can define as:

$$f_p = 1/2\pi C\left(R_X + R_{p1} R g_m\right), \tag{3.10}$$

where R_{p1} is parasitic resistance at terminals P and W_N.

Simulations were performed using commercially available active devices of VDCC shown in Figure 3.8. I implemented well-known current-mode two-quadrant multiplier EL2082 [51] (known also as electronically controllable current conveyor of second generation - ECCII) with adjustable current gain (*B*), one diamond transistor (OPA660) and current-mode four-quadrant multiplier EL4083 [52] (serving as current follower/inverter) to build VDCC. The supply voltages are selected as $V_{DD} = -V_{SS} = 5V$. Equation for equivalent capacitance available from behavioral model has form:

$$C_{eq} \cong CRBg_m = \frac{CRB}{R_{d1}}. \tag{3.11}$$

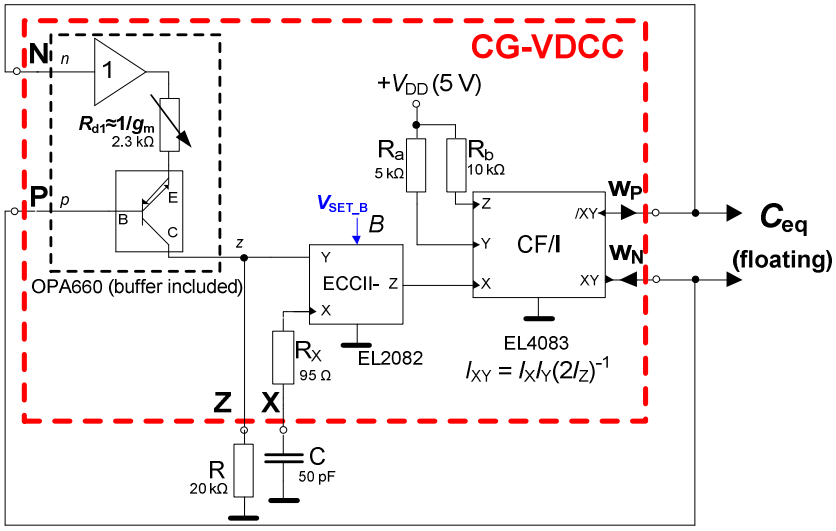
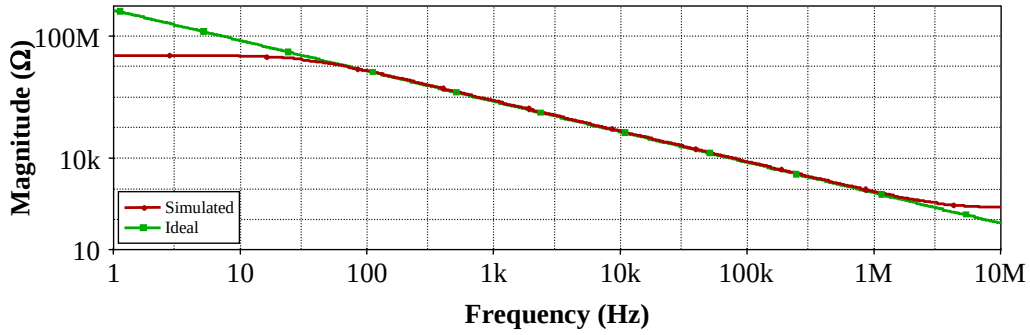
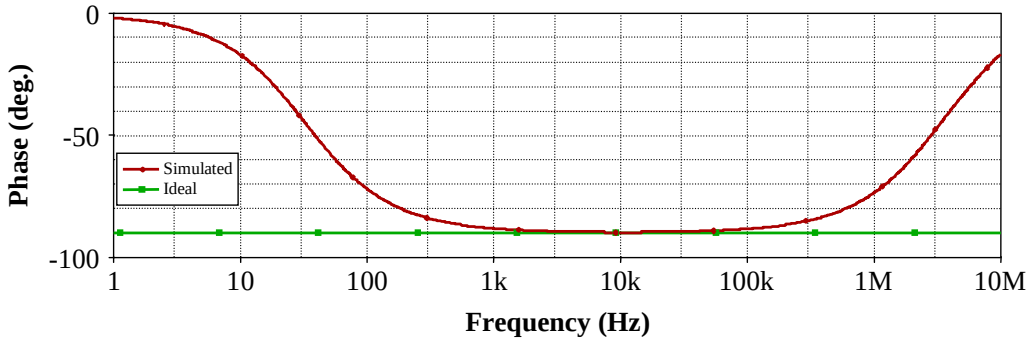


Figure 3.8 Circuit implementation with commercially available active devices

The proposed circuit shown in Figure 3.8 is simulated with the following passive element values: R_a = 5 kΩ, R_b = 10 kΩ, R_x = 95 Ω, R = 20 kΩ, C = 50 pF, B = 0.5 (V_{SET_B} = 0.5 V), where B is fine current gain adjusting, which results in C_{eq} = 220 pF. The calculation from (6) provided $R_{d1} = 1/g_m$ = 2.3 kΩ. Due to effects of parasite elements, value of B to 0.8 V was changed.



(a)



(b)

Figure 3.9 Magnitude and phase characteristics of the simulated capacitance multiplier using the behavioral model

The ideal and simulated impedance magnitudes and phase versus frequency for the proposed capacitance multiplier of Figure 3.8 are shown in Figure 3.9. It can be seen that the simulated and ideal response are very close to each other in the frequency range of 100 Hz to 1 MHz.

3.2.3 Inductance Simulator

Inductor simulators applications are in many electronic circuits such as filters, oscillators, biasing and impedance matching. Their electronic tunability by means of a voltage or a current source, high quality factor and wide frequency range of operation make them attractive with respect to physical inductors. On the other hand, many inductor simulators constructed with active building blocks such as operational amplifiers [57], second-generation current conveyors [9], current feedback operational amplifiers [58], and many CMOS-based active inductors [59] which are employed in different applications can be found in the literature.

In this chapter, the floating inductance simulator will be explained according to equation (3.1) where the basic circuit is defined in [41]; $Y_1 = G_1$, $Y_2 = G_2$ and $Y_3 = sC_3$, the input admittance becomes:

$$[Y_L] = \frac{\alpha_1\beta_1}{\alpha_2\beta_2}\frac{G_1G_2g_{m1}}{sC_3g_{m2}}\begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix}, \tag{3.12}$$

which represents a FI whose inductance is given by $L_f = \frac{\alpha_2\beta_2}{\alpha_1\beta_1}\frac{C_3g_{m2}}{G_1G_2g_{m1}}$. In ideal conditions $L_{f-ideal} = \frac{C_3g_{m2}}{G_1G_2g_{m1}}$.

The proposed circuit shown in Figure 3.1 is simulated with the following passive element values and using CMOS implementation of VDCC given in Figure 2.2: $R_{C1} = 1/G_{C1} = 200\ \Omega$, $R_{C3} = 1/G_{C3} = 1\ k\Omega$, $C_C = 780$ pF to obtain the $C_2 = 3.9$ nF in grounded form. During simulations the biasing current I_B was chosen as 63 μA, which results g_m equal to 501.5 μS. Transconductances (g_{m1} and g_{m2}) and bias currents are calculated for VDCC-I and VDCC-II $I_{B1} = I_{B2} = 63\ \mu A$ while $g_{m1} = g_{m2} = 501.5\ \mu S$.

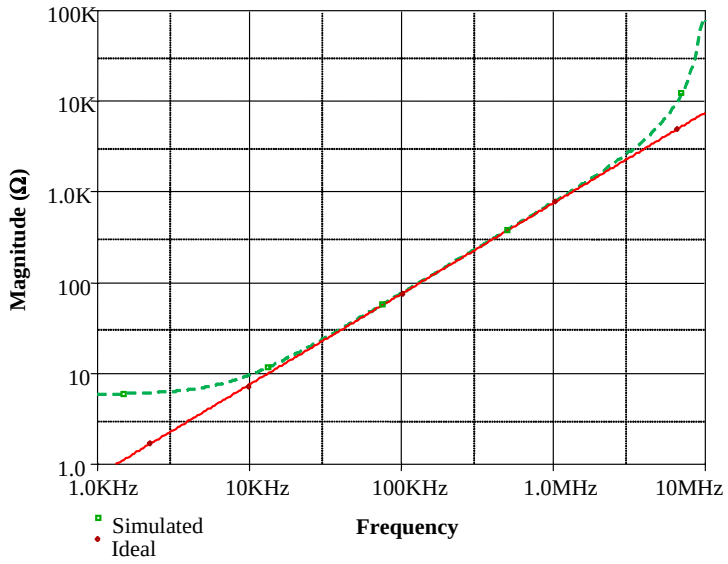


Figure 3.10 Ideal and simulated inductance simulator magnitude (impedance) response

3.2.4 Resistor Simulator

In this chapter, the floating inductance simulator will be explained according to equation (3.1); if $Y_1 = G_1$, $Y_2 = G_2$, and $Y_3 = G_3$ are selected, a FR is implemented as follows:

$$[Y_R] = \frac{\alpha_1\beta_1}{\alpha_2\beta_2}\frac{G_1G_2g_{m1}}{G_3g_{m2}}\begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix}, \tag{3.13}$$

where $R_f = \frac{\alpha_2\beta_2}{\alpha_1\beta}\frac{G_3g_{m2}}{G_1G_2g_{m1}}$. In ideal conditions, $R_{f-ideal} = \frac{G_3g_{m2}}{G_1G_2g_{m1}}$. The main benefit of such solution is controllable and increased value of resistance.

3.3 Filters

Filters are networks that process signals in a frequency-dependent manner. The basic concept of a filter can be explained by examining the frequency dependent nature of the impedance of capacitors and inductors. As the frequency is changed, the value of the reactive impedance changes, and the voltage divider ratio changes. This mechanism yields the frequency dependent change in the input/output transfer function that is defined as the frequency response.

Filters have many practical applications. A simple, single-pole, low-pass filter (the integrator) is often used to stabilize amplifiers by rolling off the gain at higher frequencies where excessive phase shift may cause oscillations. The biomedical

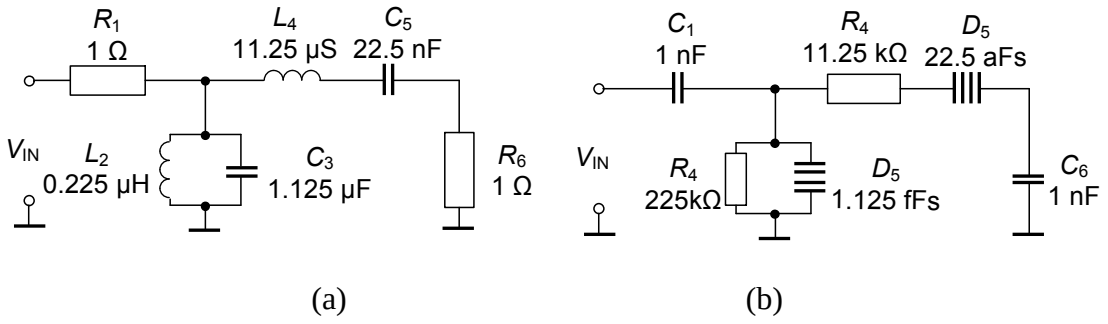
applications or sensor applications requires the low pass filters (LPFs) with very low cut-off frequency.

An all-pass filter is a signal processing filter that passes all frequencies equally in gain, but changes the phase relationship between various frequencies. It does this by varying its phase shift as a function of frequency. Generally, the first-order filter is described by the frequency at which the phase shift crosses 90°.

If a high-pass filter and a low-pass filter are cascaded, a band pass filter is created. The band pass filter passes a band of frequencies between a lower cutoff frequency and an upper cutoff frequency.

Due to the very low cutoff frequencies requirement, the filters one can use large resistance while the other can use large capacitance. Large capacitance can not be implemented on an integrated circuit because it consumes large silicon area, and also is prone to coupling noise. In large resistance design, additionally to area consumption, the power loss becomes significant. Many techniques are developed to solve this problem. Consequently, the proposed immitance simulator from Figure 3.1 has been developed as a fully differential active basic block, with LV and LP characteristics, so to be utilized in a typical application of modern integrated circuit design, that is, the implementation of floating impedance simulators, in particular high-valued capacitance multipliers and inductance simulators, so to be used in active low-pass filters and FDNR, so to be applied in active band-pass filters.

Firstly, the behavior of the FDNR circuit from Figure 3.1 has been tested in 4th-order Butterworth band-pass filter shown in Figure 3.11(a) by PSPICE simulations using CMOS implementation of VDCC given in Figure 2.2. During simulations the biasing current I_B was chosen as 63 μA, which results g_m equal to 501.5 μS.



(a) (b)

Figure 3.11 (a) RLC fourth-order Butterworth band-pass filter prototype, (b) transformed band-pass filter with FDNR [5]

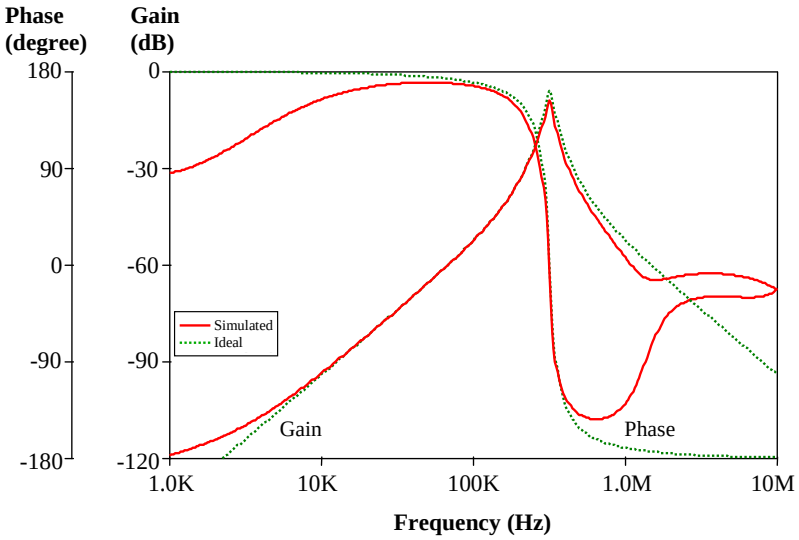


Figure 3.12 Gain and phase characteristics of the theoretical and simulated band-pass filter in Figure 3.11

The passive RLC prototype in Figure 3.11(a) has been transformed via the Bruton RLC:CRD transformation technique [55]. The required passive component values have been determined as in Figures 3.11(a) and (b). For the grounded value of FDNR and floating value of FDNR, the circuit in Figure 3.1 is chosen C_{11} = 11.254 nF, C_{12} = 1 nF, R_{13} = 100 Ω, g_{m1} = 501.5 µS to obtain grounded FDNR D_3 = 1.125 fFs, and C_{21} = 0.225 nF, C_{22} = 1 nF, R_{23} = 100 Ω, g_{m2} = 501.5 µS to obtain floating FDNR D_5 = 2.25 aFs. The 4th-order Butterworth band-pass filter bandwidth and center frequency are BW = 32 kHz and f_0 = 316 kHz respectively. Ideal and simulated responses of the transformed band-pass filter are shown in Figure 3.12.

Secondly, the performance of the floating inductance simulator and capacitance multiplier circuits from Figure 3.1 has been tested in the voltage-mode 3rd-order elliptic low-pass filter shown in Fig. 3.12. The equivalent filter employing VDCCs, resistors, and grounded capacitors-only was designed with the following specification: cut-off frequency 110 kHz, stopband frequency 205 kHz, passband ripple 1 dB, and minimum stopband attenuation 30 dB. The required passive component values have been determined as follows: $R_1 = R_2$ = 100 Ω, $C_1 = C_3$ = 27 nF, $R_{L1} = 1/G_{L1}$ = 100 Ω, $R_{L2} = 1/G_{L2}$ = 5 kΩ, C_L = 240 pF to obtain L_1 = 0.12 mH, and $R_{C1} = 1/G_{C1}$ = 200 Ω, $R_{C3} = 1/G_{C3}$ = 1 kΩ, C_C = 780 pF to obtain the C_2 = 3.9 nF in grounded form. Both ideal and simulated magnitudes of the impedances of the floating inductance simulator and capacitance multiplier and responses of the 3rd-order elliptic low-pass filter are shown in Figure 3.13.

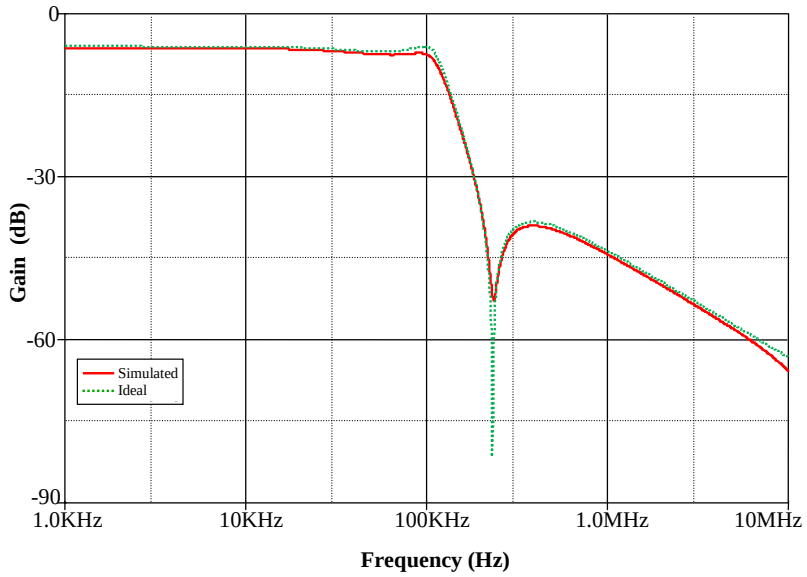


Figure 3.13 Impedance responses of the simulated gain response of the 3rd-order elliptic low-pass filter

In most cases, the amplitude response of a filter is of primary concern. Another type of filter that leaves the amplitude of the signal entire, but introduces phase shift is called an allpass filter. The aim of this filter is to add phase shift (delay) to the response of the circuit. The amplitude response of an allpass filter is 1 at each frequency, while the phase response (which determines the delay versus frequency) can be arbitrary. In other words, the phase response, however, changes from 0 to 360 (for a 2-pole filter) as the frequency is swept from 0 to infinity. Analog signal processing, automatic control systems and communication systems uses all pass filters for phase shifting applications. They are widely investigated in the literature (see [57-58] and references therein). The transfer function of an allpass filter is

$$H(s) = K\frac{1-s\tau}{1+s\tau}, \tag{3.14}$$

where K is the gain constant and its sign determines whether phase shifting is from 0 to π or from π to 0 and τ is the time constant. They have pole(s) on the left-half s-plane and zero(s) on the right-half s-plane (so-called RHP zero). Active realization of the first-order all-pass filters generally requires at least one capacitor, one resistor and active component(s). However, resistorless realization of first-order all-pass filters with electronic tunability can also be found in the literature [60], [61], [62]. Although the use of active building blocks in realization of the all-pass filters provides easy design, cascadability and low filter parameter sensitivities; they require high number of MOS

transistors which results in high power consumption and silicon area. Therefore, many efforts have been made to realize first order all-pass filters employing low number of MOS transistors [57, 60]. However, these circuits are not designed for very low-power operation. Therefore, the realization of phase shifter using uncommercial device is unsuitable for individual design and high cost consumption. The need of voltage to current (V/I) converter will obtain for input signal voltage. However, the use of V/I converter is inconvenient for most of signals in voltage form and uneconomical attraction.

The all-pass filter is designed using one OTA, differential voltage voltage buffer (DV-VB), and active voltage divider by Keskin et al. [61]. The concept of DV-VB is indirectly used also by Biolek et al. [63] where the all-pass section employs voltage differencing differential input buffered amplifier (VD-DIBA) and directly used in [64]. Here, our propose is a novel all-pass configuration which profits from the advantages of current-controlled second generation current conveyor (CCCII) and DV-VB concepts, preserving the ability of electronic control of the natural frequency as well as avoiding the use of floating passive components and DC voltage control. As a result, this filter is composed of electronically controllable current conveyor of second generation (ECCII+) [65] based on current-mode multiplier EL2082 [51], very popular diamond transistor (DT) OPA660 [49] and differential voltage buffer (DVB) AD830 [66] with unity gain transfer. DVB is very important active element for this synthesis. Simultaneous control is suitable for AP filter-based applications (phase shifters). Special magnitude and phase frequency responses suitable for advanced circuit synthesis of CPE and fractional systems are available from AP or bilinear/pseudo-AP (positive sign between absolute and linear coefficient of the numerator - zeros are in left half-plane of complex space) response, if zero frequency (ω_Z, f_Z) is adjustable separately from pole frequency (ω_P, f_P). Solutions in Figure 3.14 have this feature. Transfer function was obtained by using of Mason rule [67] and for this type of circuit, shown in Figure 3.14, is very simple:

$$K_{AP}(s) = \frac{V_{OUT}}{V_{INP}} = \frac{g_{m1} - sC_1}{g_{m1} + sC_1}, \tag{3.15}$$

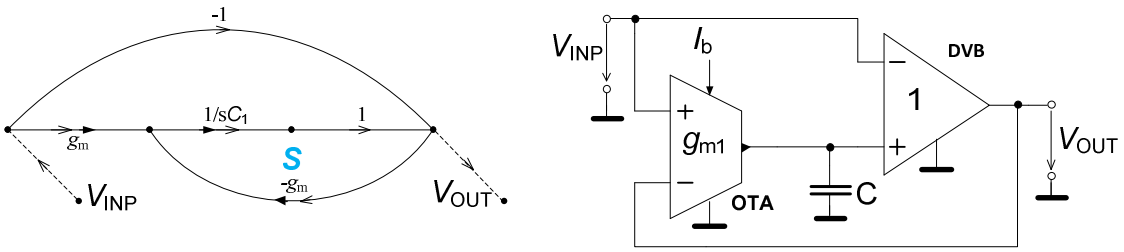


Figure 3.14 AP/bilinear section with separated zero and pole frequency control (reduced complexity of branches): a) SFG, b) circuit realization.

or:

$$K_{AP}(s) = \frac{V_{OUT}}{V_{INP}} = \frac{\frac{B_1}{R_1} - sC_1}{\frac{B_1}{R_1} + sC_1} \cong \frac{\frac{V_{SETB1}}{R_1} - sC_1}{\frac{V_{SETB1}}{R_1} + sC_1}, \tag{3.16}$$

where B_1 is adjustable current gain between X and Z terminal of the ECCII+ and $B_1 \approx V_{SETB1}$ [33]. Construction of ECCII+ is explained in Figure 3.16 (EL2082 itself represent ECCII- type, therefore output inversion is required).

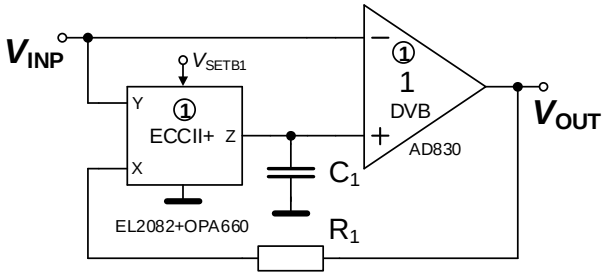


Figure 3.15 Voltage controlled all-pass section (phase shifter).

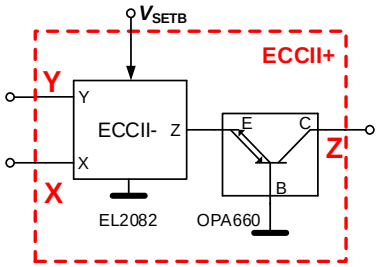


Figure 3.16 Construction of ECCII+ from ECCII- and DT.

Presented AP solution has many advantages except DC voltage control of zero/pole frequency ($\omega_{Z/P} = B_1/R_1C_1$). It offers also benefits of high-input impedance and low-output impedance and sufficiently high dynamic range.

3.4 Oscillators

Tunable oscillators with multiphase character (quadrature, for example) have many interesting various solutions. Principle of operation of known solutions can be divided to the following groups: a) lossy blocks (integrators or similar selective sections) in stepwise phase shifted cascade and full feedback (for example [68], [69] and references cited therein); b) all-pass section in combination with integrators/differentiators in simple loops ([25]-[70] for example); c) all-pass sections (APs) in the loop ([28] for example); d) other principles (see [38] for detailed discussion).

For example, the quadrature oscillator (QO) is a circuit that provides two sinusoids with 90° phase difference. Such circuit is frequently used in various applications, i.e. in telecommunications for quadrature mixers and single-sideband generators, for measurement purposes in vector generators or selective voltmeters or operating at RF bands and generating unchangeable output signals are mainly determined for applications in modern digital multi-state modulations and demodulations (quadrature phase shift keying - QPSK for example) as source of carrier signal (coherent cosine and sine wave components). Therefore, quadrature oscillators represent an important unit in many communication, control systems, signal processing, instrumentation and measurement systems

The paper of Sotner et al. [71], deals with an interesting oscillator solution derived from LC Colpitts circuit structure. The Colpitts circuit to electronically controllable system where parameters of active elements serve for frequency of oscillation (FO) and condition of oscillation (CO) control. The equivalent LC Colpitts oscillator 0 (derived from idea presented in 0 shown in Figure 3.17 have been verified by PSPICE simulations using commercially available active devices. Their solution of third-order oscillator has quadrature outputs with amplitudes independent of the tuning process and linear control of FO. One floating capacitor in the structure is a drawback which is characteristic also for standard Colpitts structure that was used for synthesis of this oscillator.

Here, our aim is replaced the remaining one disadvantage of oscillator-floating capacitor, which one comes from the principle of the Colpitts oscillator with previously defined capacitance multiplier showed in Figure 3.8.

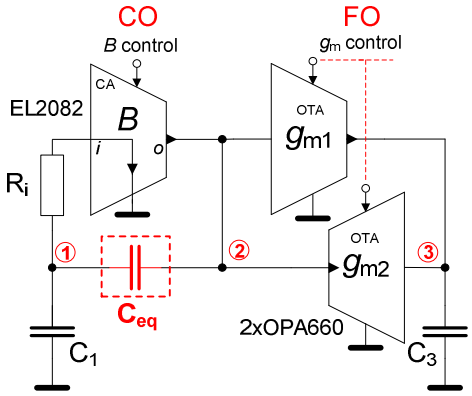


Figure 3.17 Derivation of Colpitts oscillator where floating capacitance was replaced by proposed floating C-Multiplier

Current-mode multiplier EL2082 [51] as adjustable current amplifier (*B*) and two diamond transistors (OPA660 047) to build operational transconductance amplifiers (OTAs) are used for implementation Figure 3.17. Recommended supply voltage for the devices is ± 5 V. Values of passive elements are selected as: $C_1 = C_3 = C_{eq} = 220$ pF, $R_i = 910\ \Omega$. Verification of correct operation is given for two discrete frequencies of oscillations. Therefore, transconductances ($g_{m1} = g_{m2} = g_m$) of the OTAs were adjusted in two discrete values (0.2 mS and 1 mS). Theoretical values of frequency of oscillation (FO) ($\omega_0 = g_m\sqrt{2}/C_0$) are expected as: 204 kHz and 1.023 MHz.

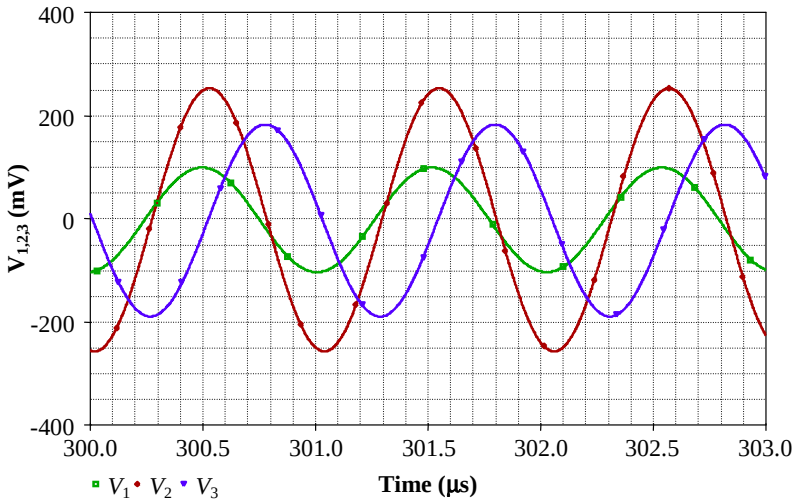


Figure 3.18 Steady state transient response of the output voltages for stable frequency

Initial setting of the oscillator was given by: $g_{m1} = g_{m2} = 1$ mS. Steady state transient responses at all three nodes (V_1, V_2, V_3) are presented in Figure 3.18 together. The FO had value $f_0 = 980$ kHz. Constant phase shift of signals V_2 and V_3 is approximately 87 degree.

Note that the V_1 is not suitable as output of the multiphase oscillator because phase shift between it and V_2 and V_1 as well as amplitude relation depends on FO 0. Nodes 2 and 3 are useful to obtain quadrature phase shift with constant amplitude level during the

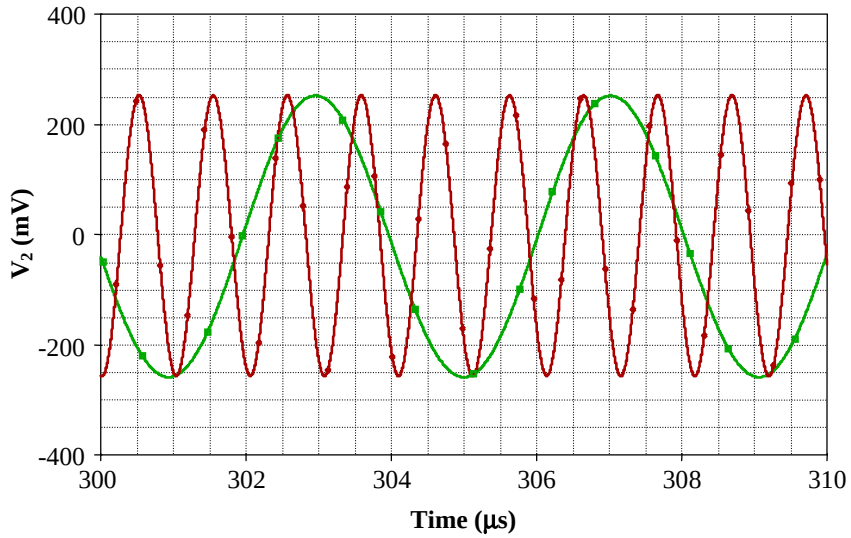


Figure 3.19 Steady state transient response for two discrere values of g_m = 0.2 (curve green) and 1 mS (curve red) at V_2

tuning process. Figure 3.19 shows steady state transient response of V_2 for oscillation frequencies 246 kHz and 980 kHz for $g_{m1,2}$ = 0.2 and 1 mS, respectively..

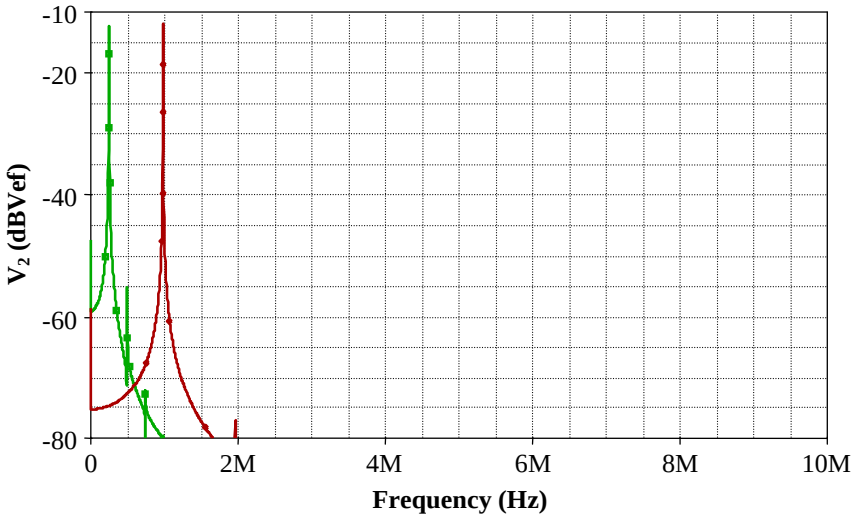


Figure 3.20 FFT spectrum of V_2 for both adjusted frequencies

FFT analysis of the output voltage V_2 is shown in Figure 3.20. Transconductance control of the commercially available active device OPA660 between 0.2 and 1 mS allows FO tuning in range from 246 to 980 kHz. Total harmonic distortion (THD) achieves values below 1% for 246 kHz (g_m = 0.2 mS) because higher harmonics components are suppressed more than 45 dBc. In the highest corner of frequency

(980 kHz for $g_m = 1$ mS), I obtain even higher suppression more than 60 dBc, that yields THD lower than 0.1% Note that frequency utilization of the C-Multiplier is restricted (see Figure 3.9) by phase error in oscillator application especially. It limits usability of our behavioral model (including specified parameters in Figure 3.8) up to 1 MHz maximally.

Problems of multiphase oscillator solutions are frequently solved in recent works For example Ozoguz et al. [73] presented utilization of functional blocks operating in approximated square-root domain for the construction of multiphase oscillator. Maundy et al. [74] used fractional-order all-pass transfer section for design of multiphase oscillator, and regarding multiphase generation based on non-standard principle was published by Promee et al. [75], where log-domain [76] approach was used to obtain reduced complexity of all-pass section, better dynamics of linear operation and wider tunability of oscillation frequency.

Our aim was designing oscillator with theoretically arbitrary phase shift of two generated signals Generation of arbitrary phase distance between two output signals was solved in simple second-order oscillator structures. The oscillator design based on two AP sections and inverting voltage amplifier presented in [38]. This solution in Figure 3.21 has many different features (includes controllable amplifier VA and different type of the phase shifters) than [38].

Base on the Barkhausen criterion, the condition of oscillation (CO) is fulfilled with $-A \geq 1$. The voltage amplifier VCA610 [77], driven by negative DC voltage, serves for control of CO. Frequency of oscillation is given by:

$$\omega_0 = \sqrt{\frac{B_1 B_2}{R_1 R_2 C_1 C_2}} \cong \sqrt{\frac{V_{SETB1} V_{SETB2}}{R_1 R_2 C_1 C_2}}. \tag{3.17}$$

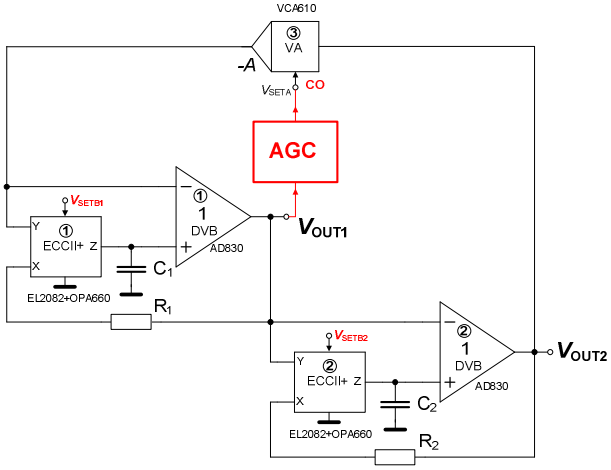


Figure 3.21 Oscillator with arbitrary adjustable phase shift.

It is clear that FO of the oscillator is linearly-electronically adjustable while $V_{SETB1} = V_{SETB2} = V_{SETB}$. The oscillator phase response can be derived from equation (3.16) where all pass filter transfer function is defined.

By routine analysis, we can obtain phase shift between input and output of the AP section (I suppose to fulfill CO $-A = 1$, i.e. gain of the inverting amplifier in positive feedback loop has to be equal to 1 at oscillation frequency). The first AP section has transfer function:

$$K_{AP1}(s) = \frac{\frac{B_1}{R_1} - sC_1}{\frac{B_1}{R_1} + sC_1} = \frac{\sqrt{\left(\frac{B_1}{R_1}\right)^2 + (\omega_0 C_1)^2}\, e^{\tan^{-1}\left(-\frac{\omega_0 C_1 R_1}{B_1}\right) j}}{\sqrt{\left(\frac{B_1}{R_1}\right)^2 + (\omega_0 C_1)^2}\, e^{\tan^{-1}\left(\frac{\omega_0 C_1 R_1}{B_1}\right) j}} = 1.exp\left[-2\tan^{-1}\left(\frac{\omega_0 C_1 R_1}{B_1}\right) j\right]. \tag{3.18}$$

Substitution of equations (3.17) to (3.18) gives phase shift (in degrees) of the AP_1 for oscillation frequency. Hence, the phase is while gain (modulus) $|K_{AP1}| = 1$:

$$\phi_{1-2} = -2\tan^{-1}\left(\sqrt{\frac{B_2}{B_1}\frac{R_1 C_1}{R_2 C_2}}\right)\Bigg|_{\substack{R_1=R_2=R \\ C_1=C_2=C}} \cong -2\tan^{-1}\left(\sqrt{\frac{B_2}{B_1}}\right). \tag{3.19}$$

It can be seen that phase shift of generated signals depends on B_2/B_1 ratio. Therefore; we can use these two parameters for electronic control of phase shift between V_{OUT1} and V_{OUT2} and for control of FO (if defined ratio is constant during the tuning process). Other parameters especially R_1 and R_2 may present for definition of phase distance (ratio) and then both identical values of $B_{1,2}$ (adjusted simultaneously) may present for FO control.

The following parameters for the oscillator in standard quadrature phase shift operation regime have been selected: $C_1 = C_2 = C = 220$ pF, $R_1 = R_2 = R = 565\ \Omega$ (470 Ω + 95 Ω of the X terminal [33]). Our design requirements are given as follows: $\varphi_{1\text{-}2} = 30$ deg in case of logic L (0 V, as explained in section 3.5.2) at the data input and oscillation frequency is $f_0 = 1$ MHz. The characteristic equation of the circuit argument from equation (3.19) can be derived as follows:

$$\frac{B_2}{B_1} = \tan\left(-\frac{\phi_{1-2}}{2}\right)^2. \tag{3.20}$$

And considering equation (3.17), we have two possibilities of driving the commutation:

$$\frac{B_2}{B_1} = \text{const.}, \tag{3.21}$$

$$\frac{B_2}{B_1} = \frac{1}{\text{const.}}, \tag{3.22}$$

while result of B_1B_2 is always the same. Therefore, we found out that the second phase distance of V_{OUT1} and V_{OUT2} (for logic H - 5 V at the data input, as explained in section 3.5.2) is given by mutual dependence of B_1 and B_2 to keep their ratio directly driving FO. We can define only initial phase distance (for logic L). The second phase distance for logic H is given by mutual dependence of equations (3.17) and (3.19). Therefore equation (3.19) or (3.20) and (3.17) does not allow to select the second phase distance, i.e. result of B_1 and B_2 have to be the same in both cases of phase shift commutation to obtain unchangeable FO. The first value of B_1 can be calculated (by substitution of equations (3.17) and (3.20)) as:

$$B_1 = \left.\frac{2\pi f_0\sqrt{R_1R_2C_1C_2}}{\tan\left(-\frac{\phi_{1-2}}{2}\right)}\right|_{\substack{R_1=R_2=R\\C_1=C_2=C}} = \frac{2\pi f_0 RC}{\tan\left(-\frac{\phi_{1-2}}{2}\right)}. \tag{3.23}$$

The calculation result is $B_1 = 2.91$ while $\varphi_{1\text{-}2} = 30$ deg. Due to nonlinear dependence of B on V_{SETB} [51] above 2 V, V_{SETB1} must be 3.4 V. The second gain/DC voltage can be expressed from equation (3.20) as $B_2 = 0.21$ ($V_{SETB2} = 0.21$ V). So I obtained two pairs of values $B_1 = 2.91$ while $V_{SETB1} = 3.4$ V and $B_2 = 0.21$ while $V_{SETB2} = 0.21$ V for logic L (data) and $B_1 = 0.21$ while $V_{SETB1} = 0.21$ V and $B_2 = 2.91$ while $V_{SETB2} = 3.4$ V for logic H from equations (3.21) and (3.22). The phase distance of V_{OUT1} and V_{OUT2} in the logic H calculated as 150 deg from equation (3.20).

3.5 Phase Shift Keying Modulator

Phase-shift keying (PSK) is a digital modulation scheme that conveys data by changing, or modulating, the phase of a reference signal(the carrier wave). A convenient method to represent PSK schemes is on a constellation diagram. This shows the points in the complex plane where, in this context, the real and imaginary axes are termed the in-phase and quadrature axes respectively due to their 90° separation. Such a representation on perpendicular axes lends itself to straightforward implementation. The amplitude of each point along the in-phase axis is used to modulate a cosine (or sine) wave and the amplitude along the quadrature axis to modulate a sine (or cosine) wave. By convention, in-phase modulates cosine and quadrature modulates sine.

In PSK, the constellation points chosen are usually positioned with uniform angular spacing around a circle. This gives maximum phase-separation between adjacent points and thus the best immunity to corruption. They are positioned on a circle so that they can all be transmitted with the same energy. In this way, the modul of the complex numbers they represent will be the same and thus so will the amplitudes needed for the cosine and sine waves.

Phase-shift keying (PSK) for fiber-optic data transmission first attracted significant attention around 1990. For practical applications, however, PSK requires precise alignment of the transmitter and demodulator center frequencies, which was difficult to achieve at the low data rates in the early 1990s. Owing to PSK's simplicity, particularly when compared with its competitor quadrature amplitude modulation, it is widely used in existing technologies. For example; the wireless LAN standard, IEEE 802.11b-1999, uses a variety of different PSKs depending on the data rate required.

The first attempt to really continuously settable phase distance of two generated signals in the frame of the simple oscillator was presented in [38]. However, no other ideas how to utilize oscillator with such feature was discussed. Therefore, presented work is focused on application of the oscillator, shown in Figure 3.21, based on all-pass filter section used for phase shift keying purposes. The circuit design is based on driving of phase commutation by data converting to two pairs of DC control voltages for control of both all-pass sections. Particular system for conversion of data to DC voltages is solved with precise amplitude automatic gain control circuit. The system operation was verified while employing commercially available devices through PSPICE program at

the modulation frequencies 1 MHz and 10 kHz with driving signals 0 V (L) and 5 V (H), respectively. Results confirmed our theoretical presumptions. The approach is continued below to jointly analyze the oscillator and all pass filter sections.

3.5.1 Proposed Design

I discussed above that all-pass filter in Figure 3.15 and continuously settable phase distance of two generated signals in the frame of the simple oscillator in Figure 3.21. However , they do not explicitly focus on how to utilize oscillator with such feature was not discussed. Therefore, I focus on simple application of the modified oscillator structure (voltage controlled all-pass sections including precise amplitude automatic gain control circuit) in simple phase shift keying modulator system including control logic (converter of data to DC driving voltages).

The PSK modulator is designed with two outputs providing identical carrier frequency and with digitally controlled phase shift between them (phase shift commutated between two values). The modification of simple oscillator based on two all-pass filtering sections [38] is used as the main building block of the solution. However, several other counterparts are required to be added to the design.

First of all, precise automatic amplitude gain control circuit (AGC) has to be designed in order to ensure and preserve stable output levels. I want to implement oscillator solution with voltage-controlled phase shift to achieve the simplest method of driving. In such a case the data (symbols) are represented by square wave with levels 0 (logic L) and 5 V (logic H). Therefore the next important task is the proposal of “converter of data (symbol) to DC control voltage”.

Therefore I divided our work to several sub-sections where all these partial problems will be discussed separately. Block structure of the system is shown in Figure 3.22.

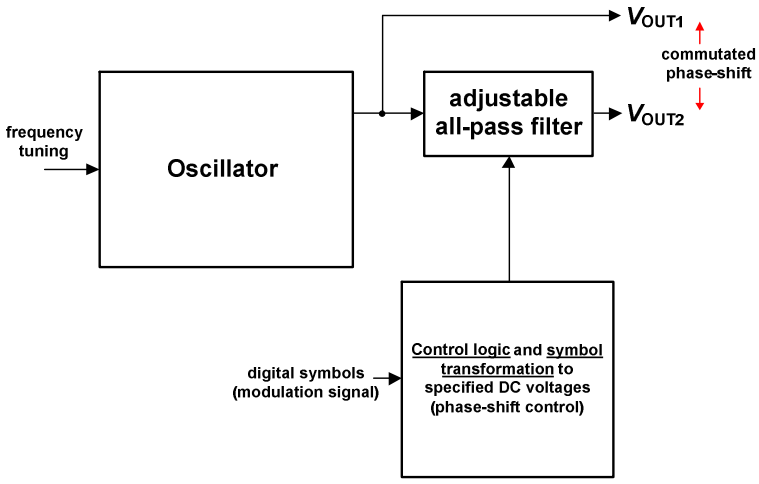


Figure 3.22 Block idea of the designed modulator.

3.5.2 Logic Control

Due to this phase shift commutation of the oscillator (see Figure 3.15) and AP blocks (see Figure 3.21), we have to ensure that two driving signals for controlling current gains $B_{1,2}$ are available when two specific values (levels) are reached. In other words, our task is designing to control logic part or "data to voltage converter" with two outputs, where two V_{SETB} (0.21 and 3.4 V) commutation is dependent on the input signal level (L or H). Therefore, the logic control circuit is designed, shown in Figure 3.23. There are two-common parts for both outputs (for V_{SETB1} and V_{SETB2}). The first part is comparator part where the detected VA output amplitude (input signal (data)) is compared with reference voltage level 1.5 V. It contains two sections/channels (for V_{SETB1} and V_{SETB2}). The first part of each channel is comparator part. The proposed logic control loop undergoes binary gain searching mode (lowest level is defined as 0 or highest level is defined as 1) and linear gain tracking mode during the comparision results between the input (modulation) signal (data) and reference level 1.5 V, which is moderated by the digital controller to decide input signal is 0 V or 5 V

In case that input level has character of log. 0, one comparator from the pair has output in high state (saturation – V_{sat_LM239} = 4.85 V) and the second in low state (0 V).

These results are evaluated by adder/subtractor based on simple opamp. The amplification/attenuation is set by resistors to ensure appropriate result of subtraction (0.21 V for L and 3.4 V for H). Therefore, DC voltage of the reference level coming to both subtraction stages is −4.85 V.

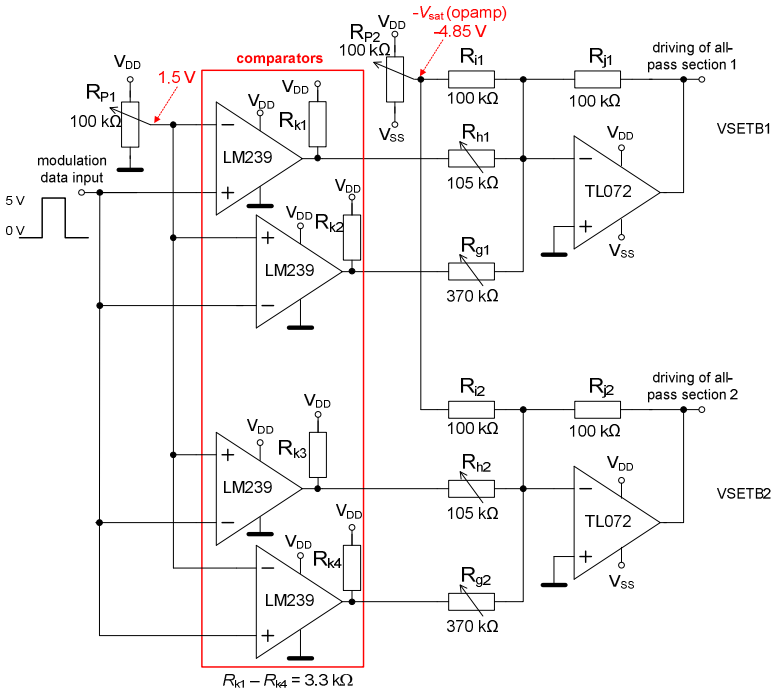


Figure 3.23 Designed converter of data symbols to DC control voltage.

Based on this, we can calculate values of resistors (resistors $R_{i1} = R_{j1}$ in the direct path with inverting unity gain were selected as 100 kΩ) of the subtractor as:

$$R_{g1} = \frac{R_{j1}}{\left(1 - \frac{V_{SETB1_L}}{V_{sat_LM239}}\right)}, \tag{3.24}$$

$$R_{h1} = \frac{R_{j1}}{\left(1 - \frac{V_{SETB1_H}}{V_{sat_LM239}}\right)}, \tag{3.25}$$

that yields $R_{g1} = 334$ kΩ (for $V_{SETB1_L} = 0.21$ V) and $R_{h1} = 105$ kΩ (for $V_{SETB1_H} = 3.4$ V). Value 334 kΩ was modified to 370 kΩ for correct setting of $V_{SETB1_L} = 0.21$ V in simulations. The second section employs the same values ($R_{h2} = R_{h1}$ and $R_{g2} = R_{g1}$) but their timing is inverted, i.e. while L causes $V_{SETB1} = 0.21$ V, V_{SETB2} has value 3.4 V and in case of H V_{SETB1} is 3.4 V and $V_{SETB2} = 0.21$ V. Simple modification of R_g, R_h values allow to set output levels of V_{SETB} quite simply.

3.5.3 Automatic amplitude gain control circuit

The typical automatic gain control (AGC) schemes are not suitable for the sinusoidal oscillator with wide oscillation frequency range. To solve this problem, an up-down

counter, multiplier, digital-to-analog (D/A) converter, and high-speed comparators are employed to achieve AGC circuit, which corrects the pair of characteristic roots of the overall system automatically to the imaginary axis of the complex frequency plane. Thus, the oscillation conditions must be satisfied to ensure that the pair of characteristic roots lies on the imaginary axis of the complex frequency plane. However, parasitic effects or parts mismatch can produce pole displacements large enough to cause the oscillation amplitude to vanish or to increase distortion severely. Therefore, an automatic gain control circuit is used to restore the oscillation amplitude to the required level with little distortion. In this sub-section, I shortly mention AGC the related discussion in sub-section 3.4.

The AGC shown in Figure 3.24 is commonly based on the paper [39]. As an application, the inertial amplitude gain control circuit is applied to a voltage - mode oscillator, shown in Figure 3.21. The AGC utilizes the peak envelope detector so diode doubler for twice higher output level and a sophisticated system of amplifiers in order to obtain a slowly altered controlling signal during comparison to FO. Response of the detector output on fluctuations in the generated signal is proportional to the time constant ($R_a||R_bC_b$). This driving signal is inverted and adjusted in level by R_c. The next stage is the DC voltage for control of CO ($V_{SETA} = -1.1$ V in Figure 3.21). Output oscillations (at AGC input) are transformed to dynamically (slowly) changing DC voltage signal from rectifier (doubler) and this signal is amplified/attenuated by inverting amplifier and summed with DC constant 1.1 V.

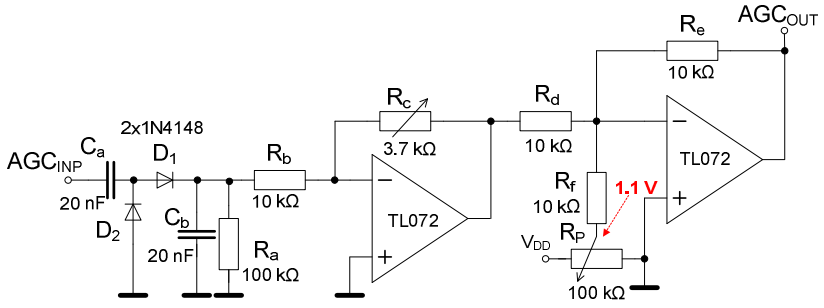


Figure 3.24 Automatic amplitude gain control circuit (AGC).

The loop gain of the overall system increases with up-count sine waveforms, decreases with down-count sine waveforms, and then approaches unity in the steady state. As a result, the pair of characteristic roots of the overall system can be automatically corrected to the imaginary axis of the complex frequency plane.

This AGC block was tested in the close-loop configuration with oscillator, shown in Figure 3.21 to see how it works in our particular case. A signal with small input amplitude is amplified to a maximal gain of 1.6 because it is too small to reach the minimal input voltage of the detector. However, increasing amplitude (sufficiently overcoming the threshold voltage of diodes in the detector), overriding approximately 550 mV, activates the AGC loop control, i.e. it creates the driving signal for subtraction with the reference DC level of 1.1 V (highlighted in red in Figure 3.24) and VA gain (see Figure 3.21) starts to be controlled by the input signal level. In other words, AGC responses on signal amplitude change by appropriate increase or decrease of the DC control voltage (V_{SETA}) for VA in Fig. 4. I tested proposed AGC applied in the oscillator where the initial parameters were defined in sub-section 3.4. This low-frequency regime of operation is chosen because of the limited frequency features of the active devices used in this design. It is always ensured for the design specifications. I focused our attention on the stability of output amplitudes and THD values during the tuning process.

3.5.4 Simulation Results

The function of the modulator system was verified in transient responses where digital input data (symbols) with frequency 20 kHz, level 0 V (L) or 5 V (H) and duty cycle 50% are directly driving the phase shift distance of both output signals (V_{OUT1}, V_{OUT2}), Figure 3.25. It also includes both driving signals from “converter of data to control voltage” used for setting of B_1 (V_{SETB1}) and B_2 (V_{SETB2}). The final result of our simulation is transient response at the both outputs of the oscillator (V_{OUT1}, V_{OUT2}). All these results are shown for FO equal to 1.055 MHz (simulated) in Figure 3.25. Detail on edge of the driving signal (data) to see the reaction of the oscillator on change of the phase distance is given in Figure 3.26.

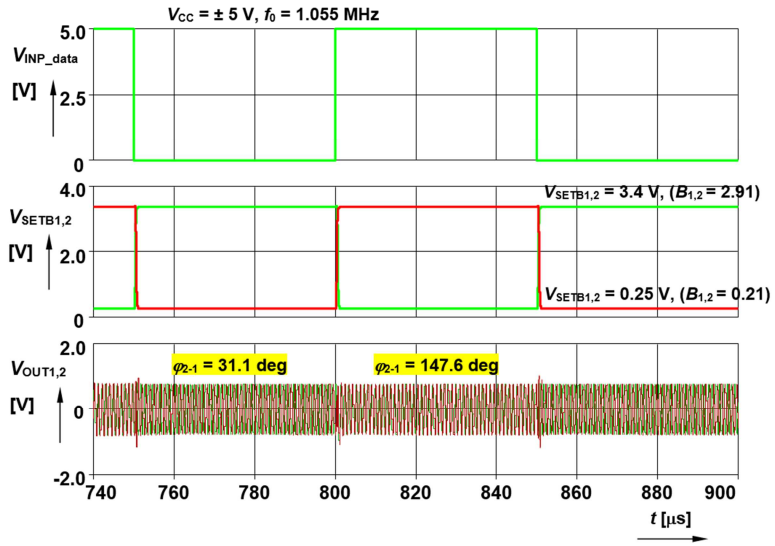


Figure 3.25 Transient response of the modulator system on the data input - phase distance commutation.

Response seems to be a little bit delayed (0.5 µs) due to the delay of the rising and falling edges of the voltages V_{SETB1} and V_{SETB2} from converter part (simple opamps with low slew rate were used in the converter in this particular solution). Stabilization of the level and waveforms takes about 1.5 µs.

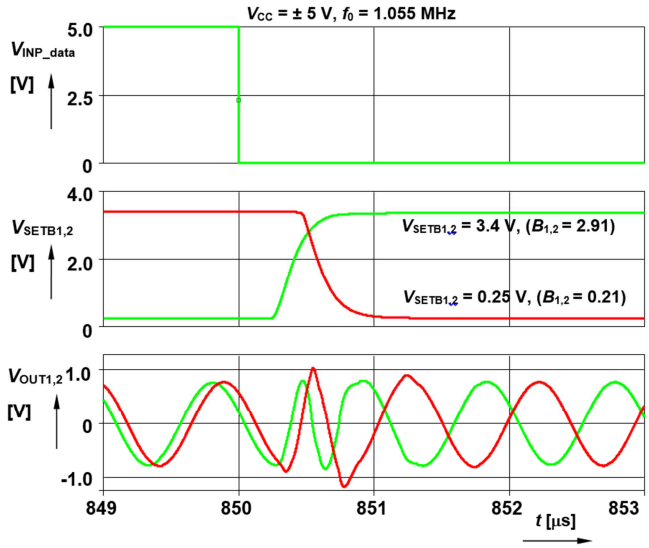


Figure 3.26 Detail on the transient effect near to falling edge of the driving signal (data) - phase distance commutation.

FFT spectrum of the output responses (V_{OUT1}, V_{OUT2}) with modulation is shown in Figure 3.27. Figure 3.28 documents spectrum of the signals without modulation. It is clear and expected that modulation causes worse phase noise features (energy is spread to wider bandwidth), as obvious from comparison of Figure 3.27 and Figure 3.28. Spectral purity of the output responses (Figure 3.28) is very high. Note that values of Y-

axis in Figure 3.27 and Figure 3.28 are in dBV (20log ($V_{OUT1,\,2}$/1 V)). Suppression of higher harmonic components is more than 60 dBc that yields total harmonic distortion below 0.1 %.

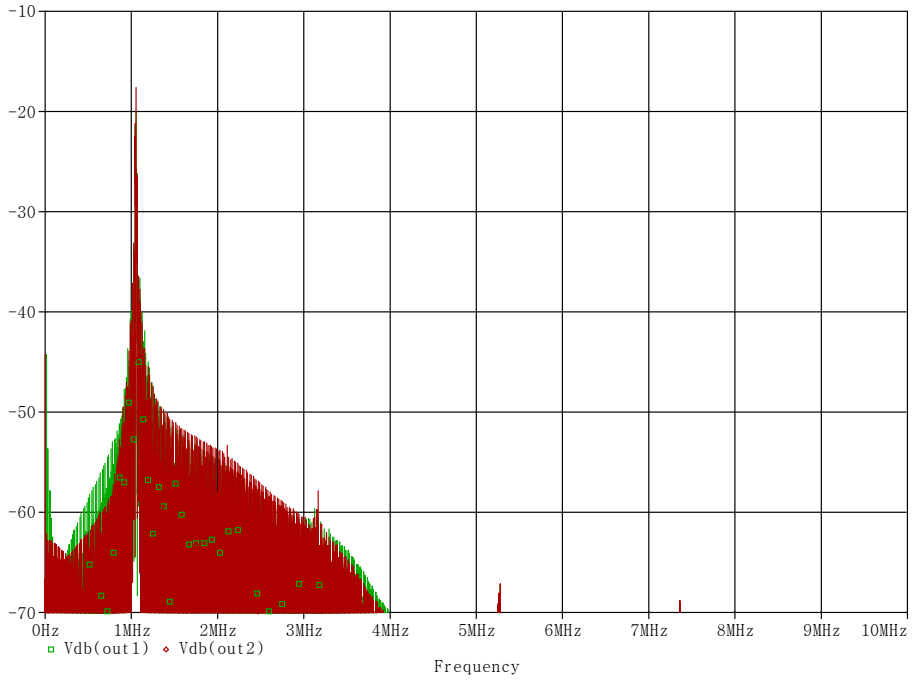


Figure 3.27 FFT spectrum of the output signals (V_{OUT1}, V_{OUT2}) under condition of modulation.

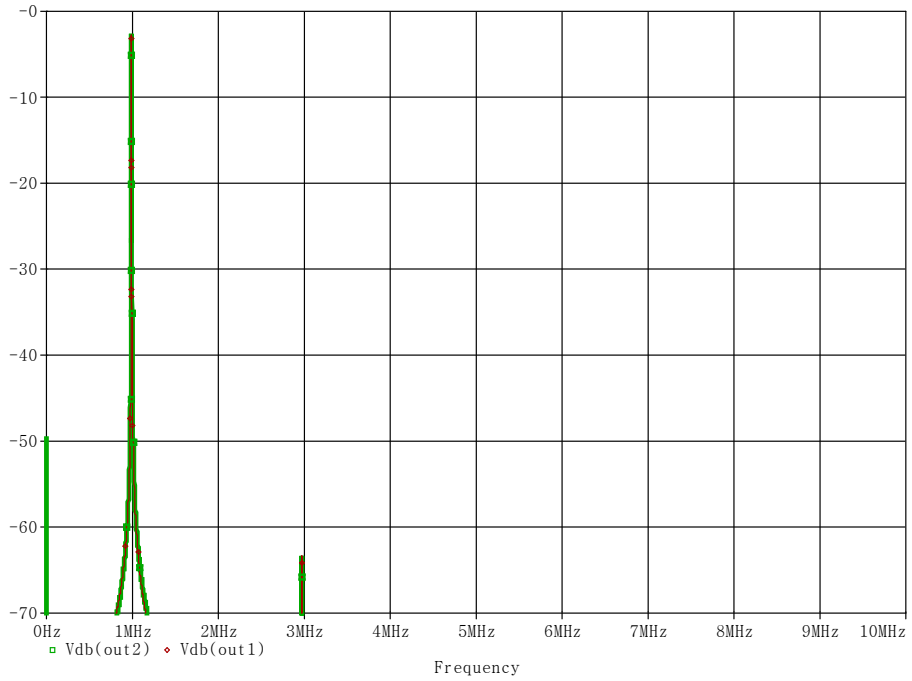


Figure 3.28 FFT spectrum of the output signals (V_{OUT1}, V_{OUT2}) without modulation.

Consequently. the results show how to utilize interesting oscillator with adjustability of the phase distance between generated signals by digital phase shift keying modulator. All required construction counterparts were carefully and detailed discussed. Design of the phase commutation was provided for initial ideal phase shift 30 degree. for input state L and frequency of oscillation equal to 1 MHz. The second ideal phase shift is 150 degree. in opposite state (assumed for H). Simulations verified and confirmed expected behavior at frequency 1.055 MHz. with two available phase shifts 31.1 and 147.6 degree. Thus, our verifications confirmed expected behavior of the system.

3.5.5 Experimental Results

To verify the behavior of the proposed phase shift modulator circuit from Figure 3.22 is designed using commercially available devices in Eagle 6.0. The working place is shown as Figure 3.29. During measurement, the modulator PCB version is photographed as in Figure 3.30.

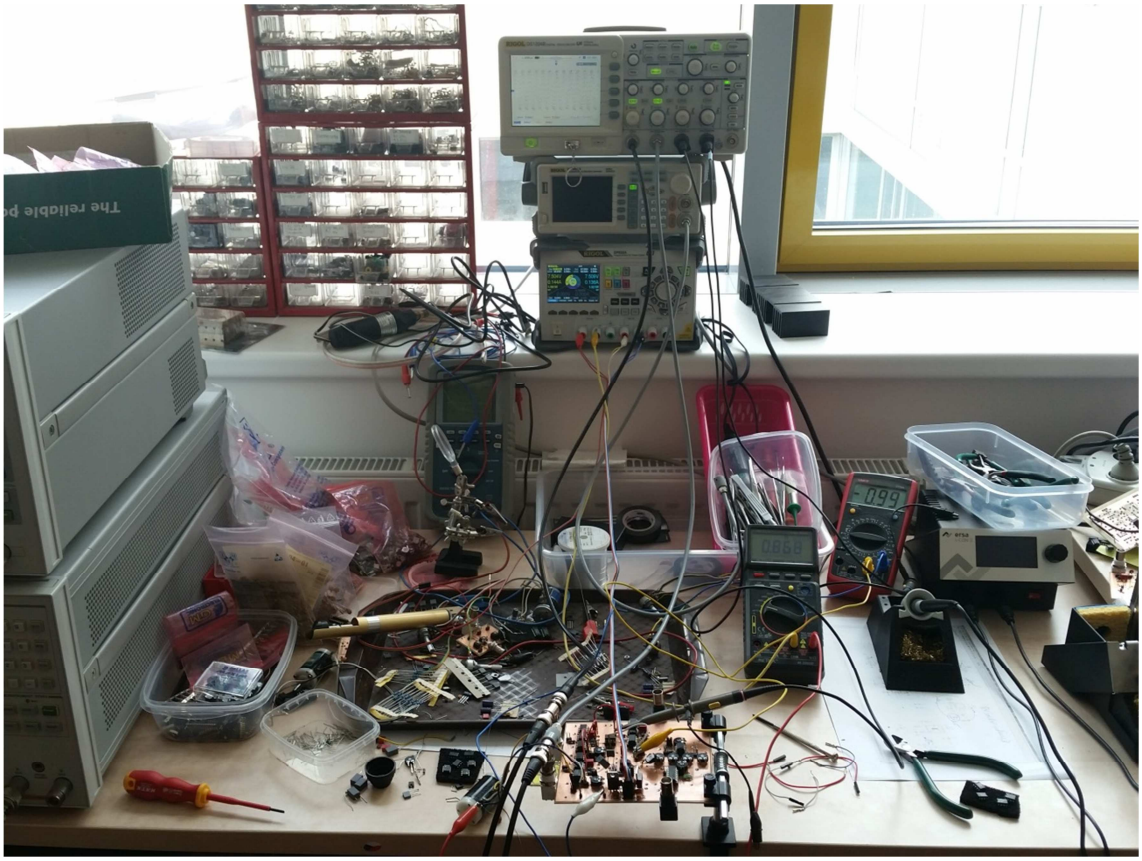


Figure 3.29 Working place during taking measurement results

Rigol DS1204B, 4 - channel, 200 MHz, 2 Gsa/s digital oscilloscope, Rigol DP832A programmable DC power supply and Agilent E5071C vector network/spectrum analyzers were used during measurement results. Many results were recorded starting from 1 kHz, because it is the lowest frequency measured by the E5071C analyzer.

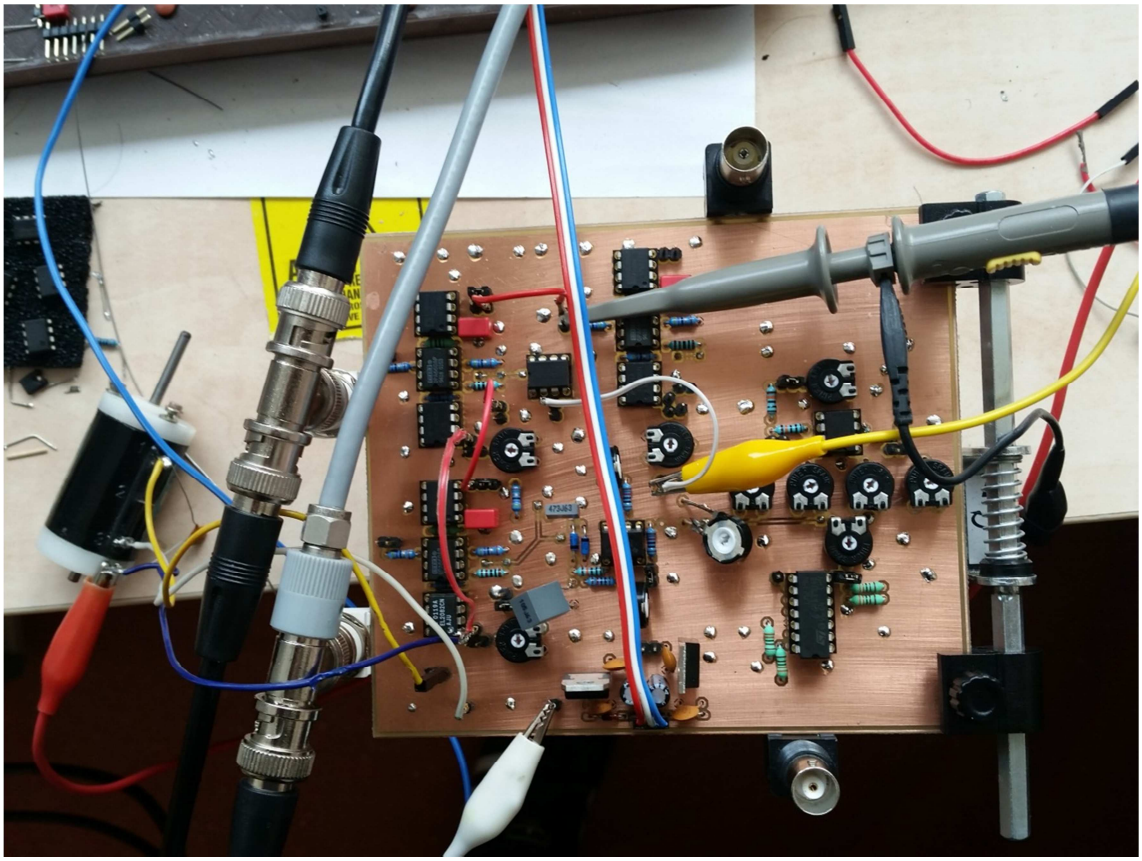


Figure 3.30 The PCB version of the designed modulator from Figure 3.22

The measurement results of PCB are taken from the both outputs of the oscillator (V_{OUT1}, V_{OUT2}). Some of these results are shown for FO near 1 MHz. Detail on edge of the driving signal (data) to see the reaction of the oscillator on change of the phase distance is given in Figure 3.31 and Figure 3.32. Tthe two driving commutation values of B_1 = 1.67 and B_2 = 0.36 is calculated on 1 MHz and 50 degree for stable design. The phase distance between two outputs is 47 degree while V_{SET2} = 1.95 V and V_{SET1} = 0.5 V and 135 degree while V_{SET2} = 0.42 V and V_{SET1} = 1.9 V.

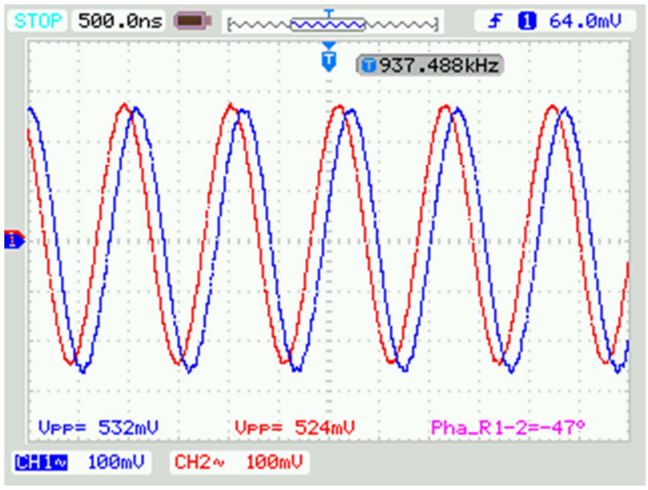


Figure 3.31 Phase distance between two outputs while V_{SET2} = 1.95 V and V_{SET1} = 0.5 V

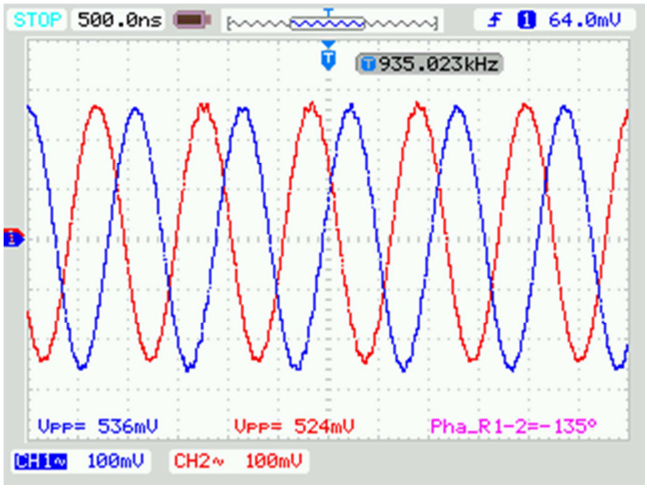


Figure 3.32 Phase distance between two outputs while V_{SET2} = 0.42 V and V_{SET1} = 1.9 V

The phase commutation between output signals at 1 kHz is shown in Figure 3.33. The commutation is from 47 degree to 135 degree as shown previous figures.

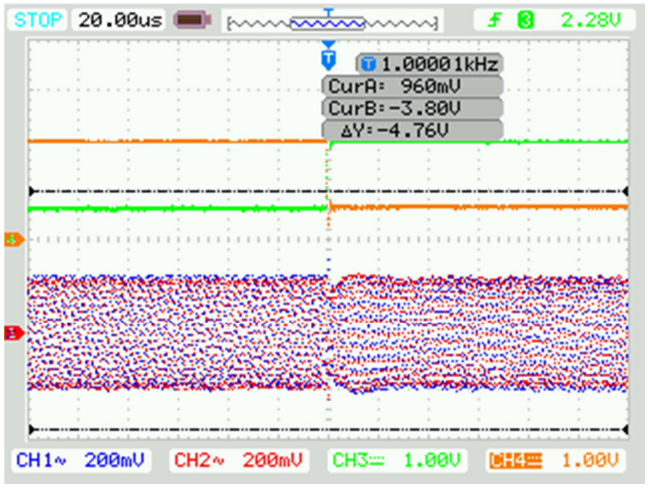


Figure 3.33 Phase commutation between output signals during modulation

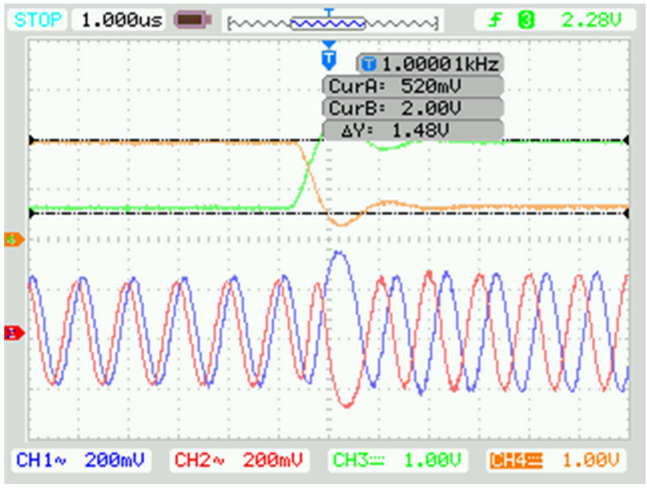


Figure 3.34 Phase modulation - detail on several period around change of input state

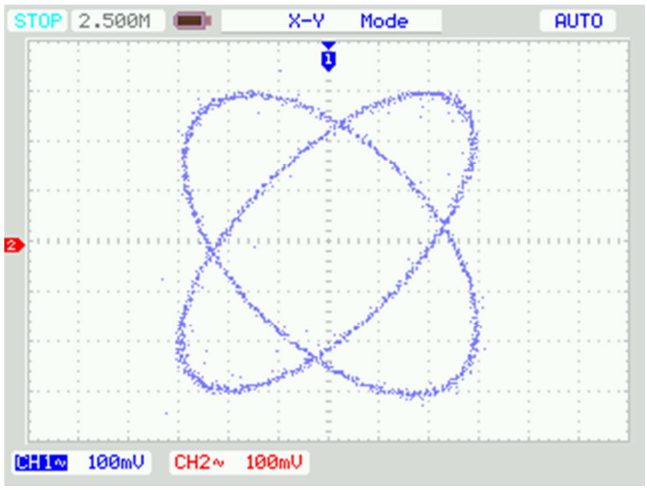


Figure 3.35 Lissajous plot

Wider time scale of operation of the modulation system in time domain is depicted in Figure 3.33. Figure 3.34 shows detail on phase shift change (output of the oscillator/modulator) in few periods around change of logic state. Both driving voltages (for oscillator) from circuit of logic control (converter of data symbols to DC voltages) are shown in upper half of the screenshot (green and brown color) and generated output signals and their phase shift was clearly catched in lower half of the screenshot. Lissajous plot in Figure 3.35 confirmed obtained phase distance of produced signals (they achieve two different phase relation – therefore two elypsoids are in Figure 3.35).

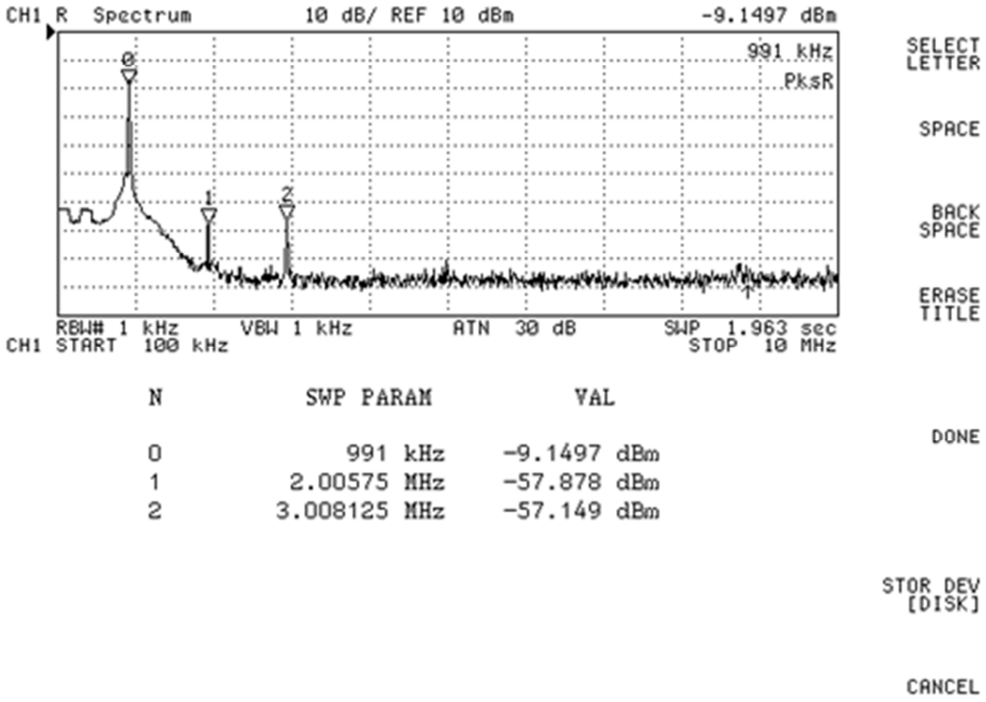


Figure 3.36 Spectrum analysis of output signal (example for V_{OUT1})

The spectral analysis of selected output (V_{OUT1}) in Figure 3.36 indicates that total harmonic distortion is deeply below 1% (distance of higher harmonic components more than 48 dBc).

CHAPTER 4

RESULTS AND DISCUSSION

Throughout this thesis, many active building blocks was covered with their commercially available equivalents and their application possibilities: voltage differencing current conveyor, current mode multipliers, different kind of operational amplifiers, quadrature differential comparators, quadrature oscillators, all pass filters, immitance simulators, phase shift keying modulation. The major target of respective integral research is to develop novel active building blocks solutions in the form of theoretical analysis and design procedure to significantly improve circuit disadvantages.

When discussing analogue building blocks such as voltage differencing current conveyor, current mode multipliers, different kind of operational amplifiers, quadrature differential comparators in Chapter 2, I repeatedly emphasized their block specification, application possibilities, literature background.

Using the proposed ABBs in Chapter 3, their applications and novel structures of first-order all-pass filters, oscillators, immitance simulators, phase shift keying are proposed.

To verify the behavior of the proposed circuits, all defined active elements are implemented using either CMOS internal structure or commercially available devices. The feasibility of selected circuits is also confirmed by experimental measurements.

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APPENDIX-A

SUMMARY OF PUBLICATIONS

Yıldız Technical University is a major public comprehensive teaching and research. The last part of this thesis includes three publications referred to as [P1]-[P3]. None of these publications were used as part of any other thesis. Additionally, the thesis refers to two important references [38] and [39] which were completed by the author in tight international collaboration with colleagues from Czech Republic. Works [P1], [P2], [P3], [38], and [39], except [P1], are papers published in international conferences as ISCAS, ECCTD, APPEL, and EUROCON.

Publications [P1], [P2], and [P3] belong to Chapter 2 and Chapter 3. Further, publications [38] and [39] relate to Chapter 3.

- **[P1]** Kartci, A., Ayten, U.E., Šotner, R., Arslanalp R., (2015). "Elektronik Olarak Ayarlanabilen VDCC Tabanli Yüzen Kapasite Carpma Devresi", Proceedings of the IEEE 23. Sinyal İşleme ve İletişim Uygulamaları Kurultayı (SIU), 16-19 May 2015, Malatya, 2369-2372.

Description

Actively simulated grounded floating capacitance multipliers have been used in several applications ranging from filter to oscillator design as well as cancellation of parasitic capacitances. In this paper, a new electronically-controllable floating lossless capacitance multiplier (C-Multiplier) circuit is presented, which employs only one Voltage Differencing Current Conveyor (VDCC), one grounded capacitor and one grounded resistor. Since the new simulated C-Multiplier uses a grounded capacitor; accordingly, it is suitable for IC fabrication. A number of simulations with employing commercially available devices through PSPICE program are accomplished to demonstrate the workability, performance, and effectiveness. Functionality of the

proposed circuit is verified through its application in a linearly tunable quadrature oscillator, which one is derived from Colpitts oscillator.

- **[P2]** Kartci, A., Ayten, U.E., Herencsár, N., Šotner, R., Jeřábek, J. and Vrba, K., (2015). "Application Possibilities of VDCC In General Floating Element Simulator Circuit", Proceedings of the 22nd European Conference on Circuit Theory and Design (ECCTD), 24-26 August 2015, Trondheim, 1-4.

Description

In this study, a low-voltage design of a new general floating element simulator circuit for realizing floating frequency dependent negative resistor (FDNR), floating inductor (FI), floating capacitor (FC), and floating resistor (FR) simulator, depending on the selection of passive circuit elements, is described. The circuit employs two voltage differencing current conveyors (VDCCs) at low voltage levels (±0.45 V) and three passive components. Moreover, the new general floating element simulator can be electronically controllable by changing the bias currents of the VDCCs or can be controlled through the grounded resistor or capacitors. Finally, using one of the described floating element simulator, i.e. FDNR, a fourth-order Butterworth characteristic band-pass filter is simulated via PSPICE using 90 nm, level 7 PTM CMOS technology parameters. One advantage of the proposed circuit is that an FDNR realization employs only grounded passive components. Furthermore, the circuit allows easy compensation for the parasitic resistances and capacitances. An application example and simulation results are included to verify the theory. The proposed implementations can be used for realizing electronically tunable large values of capacitances and resistances as well as FDNRs required for designing integrated circuit active filters *etc.*

- **[P3]** Kartci, A., Ayten, U.E., Herencsár, N., Šotner, R. and Vrba, K., (2015). "Floating Capacitance Multiplier Simulator for Grounded RC Colpitts Oscillator Design", Proceedings of the 20th International Conference on Applied Electronics, 8-10 September 2015, Pilsen, 93-96.

Description

Actively simulated grounded floating capacitance multipliers have been used in several applications ranging from filter to oscillator design as well as cancellation of parasitic capacitances. In this paper, a new electronically-controllable floating lossless

capacitance multiplier (C-Multiplier) circuit is presented, which employs only one Voltage Differencing Current Conveyor (VDCC), one grounded capacitor and one grounded resistor. Since the new simulated C-Multiplier uses a grounded capacitor; accordingly, it is suitable for IC fabrication. A number of simulations with employing commercially available devices through PSPICE program are accomplished to demonstrate the workability, performance, and effectiveness. Functionality of the proposed circuit is verified through its application in a linearly tunable quadrature oscillator, which one is derived from Colpitts oscillator.

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PUBLISHMENTS

Papers

[1] Šotner, R., Kartci, A., Jeřábek, J., Herencsár, N., Dostál, T. and Vrba, K., (2012). "An Additional Approach to Model Current Followers and Amplifiers with Electronically Controllable Parameters from Commercially Available ICs", Measurement Science Review, 12(6):255-265.

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Projects

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