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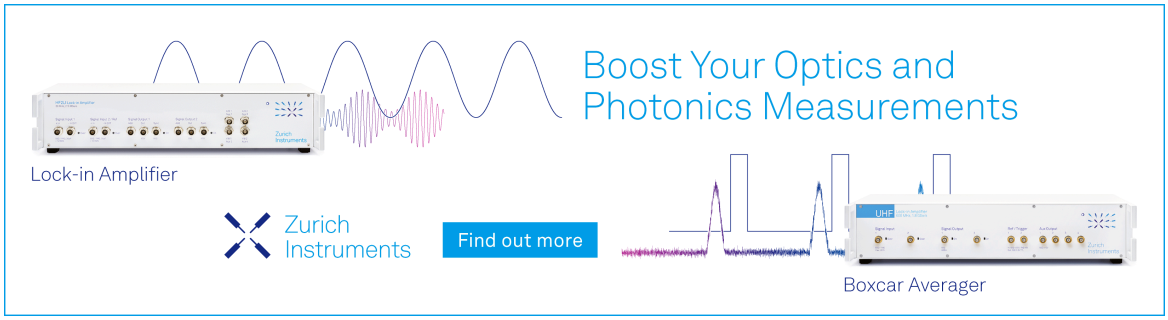

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ABSTRACT

We report on the study of electron transport and band offset across β-Ga_2O_3/4H-SiC N–n isotype heterojunction. N-type β-Ga_2O_3 of thickness 2.7 μm was grown using low-pressure chemical vapor deposition using germanium (Ge) as the dopant on an n-type 4H-SiC substrate. The grown epilayer having (−201) orientation was verified through XRD. Temperature-dependent I–V and C–V measurements were performed (50–300 K) to investigate the transport properties across the heterojunction. First, lateral diodes were fabricated on β-Ga_2O_3, and from C–V, n-doping was estimated to be 2.3×10^{17} cm^{-3} in the epilayer while the Schottky barrier height was estimated to be 1.75 eV. In top-down I–V sweeps, the reverse current across the heterojunction exhibited marginal dependence on temperature, indicating a possible tunnelling-based transport mechanism, while the forward current exhibited an exponential dependence on both temperature and the applied bias. The band diagram indicated the formation of a two-dimensional electron gas (2DEG) at the hetero-interface, which was indirectly confirmed using C–V measurement and TCAD simulation at low temperatures. From the position of the Fermi level in SiC and band diagram, a conduction band offset of 0.4–0.5 eV was estimated between β-Ga_2O_3 and 4H-SiC.

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I. INTRODUCTION

Beta gallium oxide (β-Ga_2O_3) is gaining significant traction among material and device communities as it is an attractive candidate for high-voltage power devices owing to its excellent critical breakdown field of 8 MV/cm.[1] Although the availability of single-crystal bulk β-Ga_2O_3 wafers makes it quite promising for the economy of scale besides assuring superior structural quality, heteroepitaxial growth of β-Ga_2O_3 is attractive for several reasons. First, it enables heterojunction, which could lead to novel and/or high-performance vertical devices. Second, given the high cost of single-crystal β-Ga_2O_3 wafers, heteroepitaxial growth offers the possibility of a low-cost epitaxial. Third, the heteroepitaxy of β-Ga_2O_3 on high thermal conductivity substrates such as SiC would help address the heating issues of high-power devices, a serious concern otherwise, considering the extremely poor thermal conductivity of β-Ga_2O_3.[2] There are a few other advantages of heteroepitaxial β-Ga_2O_3, such as growth on sapphire can enable back-illumination for deep-UV detectors, growth on silicon can lead to ease of integration with CMOS and/or the use of CMOS fab for scalability, etc.

However, studies of heteroepitaxial β-Ga_2O_3 are still at a nascent stage, and particularly, few reports exist on β-Ga_2O_3/SiC[3–7] heterostructure. β-Ga_2O_3 on p-type 4H-SiC heterojunction has been studied for its application in deep UV as a photodetector,[3] while some reported on the effect of oxygen vacancies on the photoresponse from such junction.[5] While a few reports focused on the electrical and optical behavior of such junctions, most of the works are oriented toward understanding the thermal behavior of such heterostructures, where the high thermal conductivity of 4H-SiC can be exploited to improve the device's performance.[6,7] At the same time, while the growth of β-Ga_2O_3 for device application is usually reported using metal-organic chemical vapor deposition (MOCVD), molecular beam epitaxy (MBE), mist-CVD, and pulsed laser deposition (PLD) (laser MBE),[8–10] there are very few studies on the low-pressure chemical vapor deposition (LPCVD) growth of β-Ga_2O_3[11–14] on 4H-SiC. Out of these, most are primarily concerned with understanding the growth strategies of $\beta-Ga_2O_3$ on 4H-SiC[11–13] and on the bonding characteristics between these two materials.[14] Industrially scalable LPCVD growth of Ge-doped

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β-Ga_2O_3 can be achieved using elemental Ga and Ge sources and O_2 gas source, thus avoiding hazardous and expensive gas-based metal or dopant precursors.[15] There have been no recent reports on the study of β-Ga_2O_3/4H-SiC heterostructure grown via LPCVD with a focus on characterizing the heterojunction. In this letter, we report on the study of electron transport across an N–n isotype heterojunction formed between LPCVD-grown Ge-doped β-Ga_2O_3 and 4H-SiC. We study the temperature-dependent I–V and C–V of the isotype diode, compare the data with that obtained from TCAD simulation, and estimate the band offset between the two materials to be 0.4–0.5 eV. This study of heterojunction of β-Ga_2O_3 on thermally and electrically conductive substrates such as SiC is expected to create a new paradigm in vertical devices

II. EXPERIMENT

A. Material growth and characterization

The substrate used in the study is 350 μm thick, nitrogen-doped, n-type 4H-SiC with 4° offcut toward $\langle 11-20 \rangle$. It has a specific resistivity of 0.02 Ω cm and an n-type doping concentration of 3×10^{18} cm^{-3} as per the specification provided by the commercial vendor. The details of the growth system have been reported previously.[12] The substrate and a quartz crucible with a 7N purity Ga source were placed in the first heating zone with 2.5 cm spacing, and the temperature of the zone was set to 900 °C. Another quartz crucible with a 5N purity Ge source was placed in the center of the third zone, and the zone temperature was set to 800 °C. The oxygen and argon flow of 2 and 500 sccm was set, respectively. The growth pressure was measured to be 2 Torr by a digital manometer located near the pump side of the quartz tube. The growth was carried out for 3 h under the given growth conditions. The thickness of the epitaxial β-Ga_2O_3 layer is 2.7 μm thick, confirmed through SEM cross-sectional imaging. Figure 1(a) shows the AFM image of the Ga_2O_3 surface. The rms roughness of the surface is 22 nm. The surface roughness is better than a few of the reports,[16] while a relatively higher surface roughness compared to other growth techniques, such as MOCVD[7] and MBE,[17] can be attributed to the higher growth rate (900 nm/h) for this sample. The epitaxial β-Ga_2O_3 has (−201) orientation, as confirmed by the XRD data in Fig. 1(b). Since the XRD was done after device fabrication, Ti and Au peaks can be seen in Fig. 1(b), which are on the film's top surface. The family of (−201) peaks further confirms that there has been no change in the crystallinity of the sample after the fabrication process. The SEM image of the as-grown surface is shown in Fig. 1(c).

B. Fabrication process

The sample, 1 × 1 cm^2, was cleaned in the standard Piranha solution (3:1 H_2SO_4:H_2O_2) for 5 min. The backside Ohmic contact on carbon-faced SiC was patterned with Ni/Au (100/20 nm) through standard lithography and liftoff process. The contacts were annealed through an RTP process of 1050 °C for 1 min in N_2 ambient to ensure the formation of Ohmic contact.[18] The TLM characterization on the 4H-SiC substrate yields a sheet resistance of 131 Ω/□ and a contact resistance of 0.61 Ω mm. On the epi-surface of β-Ga_2O_3, we deposited Ti/Al/Ni/Au (50/100/30/50 nm) stack to form Ohmic contact as well as Ni/Au (50/100 nm) to realize Schottky contact.[19] For this, first, lithography was done to pattern for Ohmic contacts, some of which were circular pads to enable top-down measurements, and others were annular rings. The sample was dipped in 1:5 HCl:DI water solution for 30 s to clean the surface pre-metal deposition. An RTP annealing was performed at 500 °C for 1 min in N_2 ambient after Ohmic stack deposition.[19] Next, circular patterns were made for Schottky contact such that these pads are inside the annular rings: this enables us to realize lateral Schottky diodes on the β-Ga_2O_3 surface. Figures 2(a) and 2(b) show the cross-sectional schematic and the microscopic images of the device, respectively. The circular Schottky pads are 100, 150, and 200 μm in diameter. The TLM measurement of the front side gave the sheet resistance and contact resistance values to be 42 K Ω/□ and 200 Ω mm, respectively. The sheet resistance could be overestimated as the contact formed is not purely ohmic. However, the I–V characteristic is linear for the desired range of measurement. Figure 3 shows the I–V characteristic between two TLM pads (100 × 100 μm^2) with a spacing of 4 μm between them. The inset to Fig. 3 shows the resistance vs distance profile for the TLM measurement carried for a temperature range of 50–300 K.

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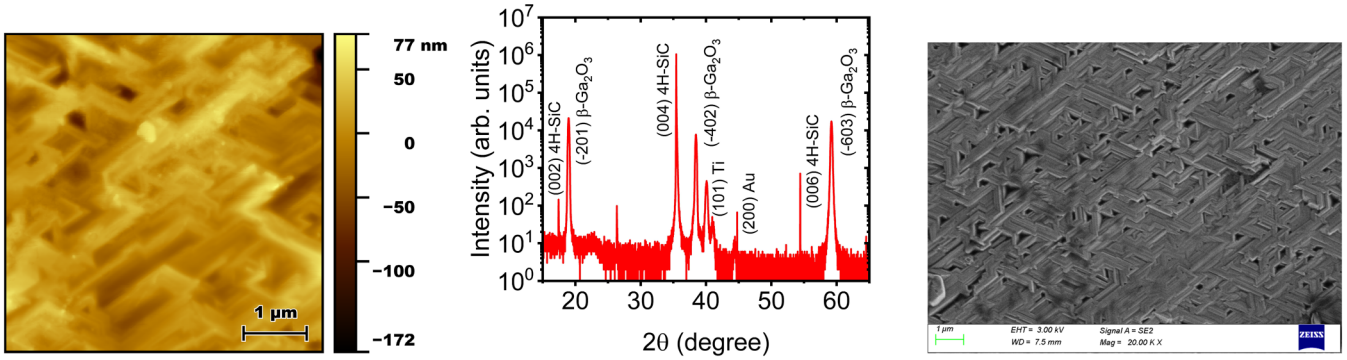

FIG. 1. (a) AFM scan of the epitaxial layer; (b) 2θ XRD scan indicating the (-201) orientation of the epitaxial layer; and (c) SEM image of the epitaxial layer.

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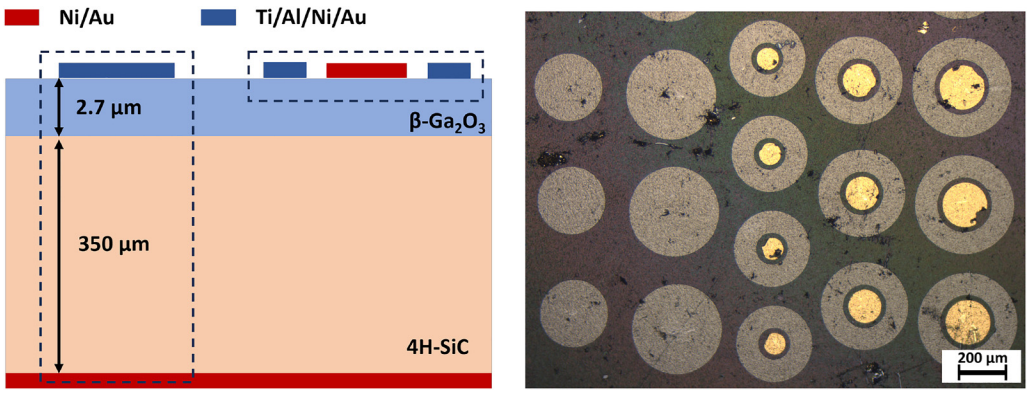

FIG. 2. (a) Cross-sectional and (b) microscopic image of the fabricated device.

The points obtained were linear, and the fit to it derived the contact resistance in the range of 2035–200 Ω mm for the temperature range of 50–300 K.

III. RESULTS AND DISCUSSION

The lateral C–V measurement characterizes the front doping density of the Ga_2O_3 layer through the lateral Schottky structures. Figure 4 shows the C–V plot obtained. The built-in potential and barrier height of the Schottky interface are determined from the C–V plot using the equation[20]

$$\frac{1}{C^2} = \frac{2}{q\varepsilon_s N}\left(V_{bi} - V_R - \frac{2KT}{q}\right), \tag{1}$$

where V_R is the reverse voltage and ε_s of $10\varepsilon_o$ is considered for Ga_2O_3.[21,22] The value of the built-in potential V_{bi} and the doping density N can be estimated from the intercept and slope of the $\frac{1}{C^2}$ vs V plot,[23] as shown in the inset in Fig. 4. A V_{bi} of 1.68 eV and doping density of 2.3×10^{17} cm^{-3} was extracted for the Ga_2O_3 layer. Furthermore, the Schottky barrier height can be estimated as the sum of the built-in potential and the Fermi potential with respect to the conduction band ($E_C - E_F$). From the doping density derived using the linear fit, the value of $E_C - E_F$ can be estimated using Eq. (7). Adding the value of V_{bi} and $E_C - E_F$, we derive the Schottky barrier height, ϕ_B, of 1.75 eV.

Incorporating the doping densities for Ga_2O_3 and 4H-SiC, the equilibrium energy band diagram of the heterojunction was obtained using Silvaco TCAD simulation. The structure was simulated under equilibrium conditions. Figure 5 shows the band structure of the heterointerface at 300 K. The inset to Fig. 5 shows the conduction band discontinuity and the position of the Fermi level under equilibrium. The material properties of Ga_2O_3 were defined as the simulator does not have the in-built library for Ga_2O_3, unlike 4H-SiC. We define the electron affinity of 4.0 eV,[24] the bandgap of 4.8 eV,[14] the conduction band density of states of 3.7×10^{18} cm^{-3}, the permittivity of 10,[21,22] and the thermal

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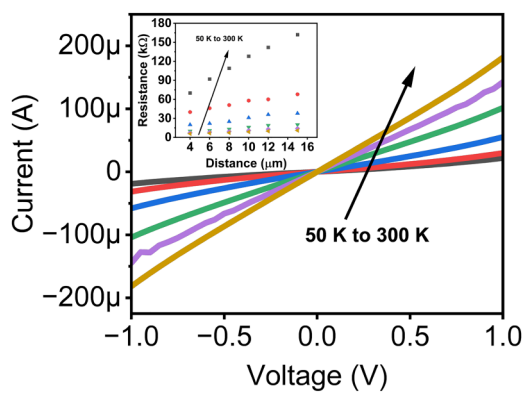

FIG. 3. I–V plot for different temperatures. The inset shows the TLM fit to obtain the contact resistance.

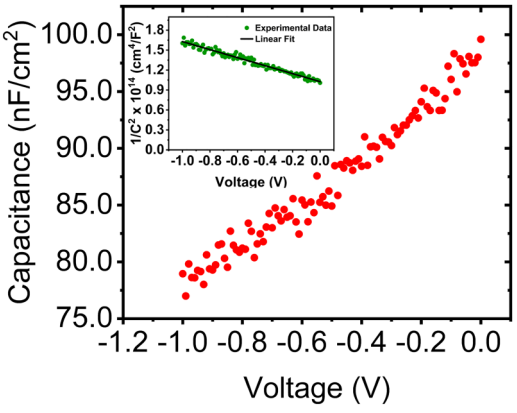

FIG. 4. C–V plot from the lateral measurement. The inset shows $\frac{1}{C^2}$ vs V fit to derive barrier height.

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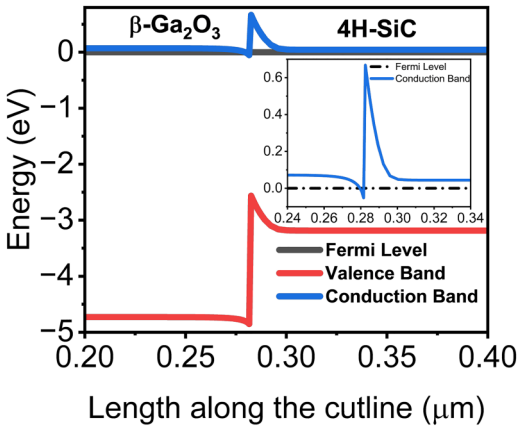

FIG. 5. Heterojunction equilibrium band diagram at 300 K. Inset shows the conduction band energy profile near the hetero-interface.

conductivity of 0.13 W/cmK.[2] On the other hand, standard material parameters embedded in the software were used for 4H-SiC. We incorporated the Boltzmann model to account for the distribution of carriers at various temperatures and employed Newton's method to solve the mesh points and obtain the band diagram.

The band diagram shows the possibility of a 2DEG on the Ga_2O_3 side at the Ga_2O_3–SiC interface. Such energy landscapes at the interface have previously been reported for n-type Ga_2O_3 and n-type 4H-SiC and 6H-SiC interfaces.[5,25]

Figure 6 shows the temperature-dependent I–V characteristic of the device. Forward and reverse I–V characteristics were measured between the top and bottom contact (Ohmic–Ohmic). For vertical measurements, the top contact on the Ga_2O_3 was biased with respect to the bottom contact.

To understand the transport mechanism in forward bias, we employed the thermionic emission (TE) model, which is the most commonly observed mechanism for electrons traversing a barrier[26] and usually reported for Ga_2O_3-based diodes.[27] The equation governing the thermionic emission model is given as[20,27]

$$J = J_0\left(\exp\left(\frac{qV}{\eta KT}\right) - 1\right), \tag{2}$$

$$J_0 = A^* T^2 \exp\left(\frac{q\phi_B}{KT}\right), \tag{3}$$

where $A^* = 146$ for SiC[28] is taken in the above equation because the depletion exists on the SiC side, and electrons from SiC traverse the barrier to reach the other end. K is the Boltzmann constant, ϕ_B is the barrier height of the heterojunction, and J_0 is the reverse leakage current. Considering V¿3KT and taking natural logarithm on both sides, the above equation can be written as

$$ln(J) = ln(J_0) + \left(\frac{qV}{KT}\right). \tag{4}$$

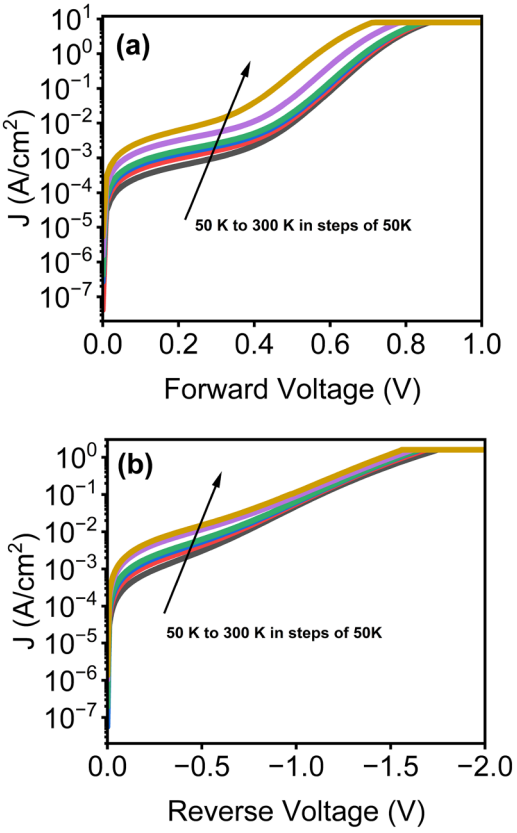

FIG. 6. Temperature-dependent I–V characteristic in (a) forward bias and (b) reverse bias.

From the linear fit of the plot of $ln(J)$ vs $\frac{V}{KT}$ as shown in Fig. 7, the reverse saturation current and the ideality factor can be derived from the intercept and slope of the linear fit, respectively.

Once the reverse saturation current is derived, the barrier height can be derived from Eq. (3). However, upon close examination, the reverse saturation current does not have an exponential relationship with the temperature, as shown in the inset in Fig. 7. Also, the derived barrier height and ideality factor (>4) are impractical in this temperature range, suggestive of the fact that thermionic emission is not the desired transport mechanism in the forward bias. The diode current, however, shows an exponential dependency on voltage and temperature, which have been previously reported with the equation of the form[29,30]

$$J = B \times \exp(A_I V \times \gamma T), \tag{5}$$

where B depends on the tunnelling probability, A_I is a temperature-independent constant, and γ reflects the temperature dependence of the bandgap. Figure 8 shows a plot of current density as a function of temperature. The straight line has an almost equal slope at lower bias values. This suggests temperature

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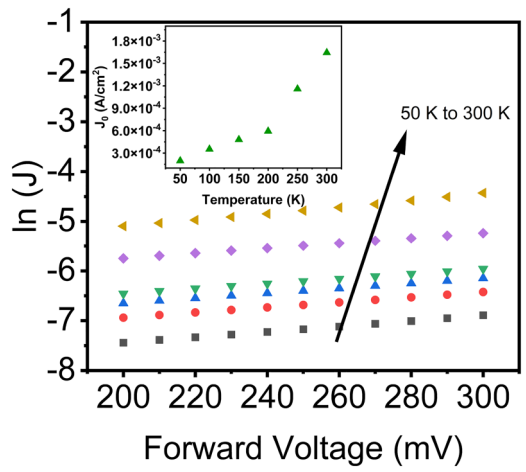

FIG. 7. Linear fit for the TE model. Inset shows reverse saturation current as a function of temperature.

independence of A_I. Also, the linear nature of the plot suggests that the current varies exponentially with temperature, as suggested in Eq. (5) above. On the other hand, the weak temperature dependency of the reverse current, as seen in Fig. 6(b), suggests a tunnelling mechanism, which is evident due to the thin depletion barrier on the SiC side.

Next, capacitance–voltage measurements were carried out for a temperature range of 50–300 K, as shown in Fig. 9.

The zero bias depletion width was extracted from the C–V measurement at different temperatures. Considering the presence of 2DEG, the region from the top contact to the 2DEG and the bulk of SiC essentially act as the top and bottom contacts, respectively. Thus, the capacitance measured is due to the small depletion at the heterojunction on the SiC side. The zero bias depletion

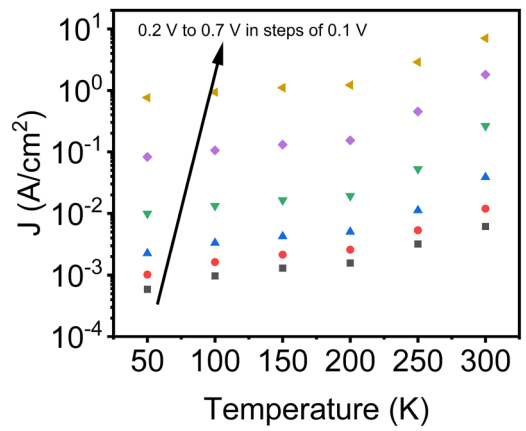

FIG. 8. Current density as a function of temperature for different forward bias voltages.

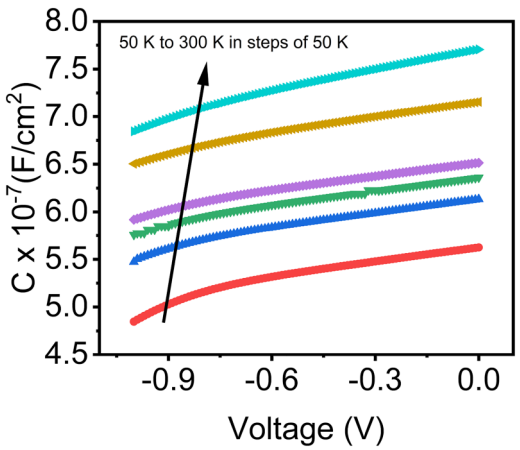

FIG. 9. Temperature-dependent C–V characteristic of the vertical device.

width extracted from the C–V measurement is in good agreement with the simulated result. The decrease in depletion width with the increase in temperature is suggestive of the increase in the carrier concentration, as shown in Table I. The built-in potential was extracted via an indirect method. Considering 100% ionization of carriers at 300 K, the doping density of SiC is considered the charge carrier density. The fractional reduction in the capacitance can be attributed to the reduction in the charge density as $Q = CV$. Thus, the fractional ionized charges can be calculated from the measured C–V data at a given temperature. The zero bias depletion width and the carrier concentration have been listed in the table below.

Once the carrier concentration is calculated, the built-in potential can be calculated using the expression[20]

$$V_{bi} = \frac{qNx_d^2}{2\varepsilon_s}, \tag{6}$$

where N is the carrier concentration of the 4H-SiC at different temperatures obtained in Table I, and ε_s is 9.6 for 4H-SiC,[31] with x_d being the depletion width listed in Table I. Since the carrier concentration at different temperatures is given, the relative position of the Fermi level, E_F, with respect to the conduction band energy E_C

TABLE I. Built-in potential and fermi potential for different temperatures extracted from the C–V measurement.

Temperature (K)	Depletion, x_d (nm)	Carrier density, N (cm^{-3})
50	15.7	2.19×10^{18}
100	14.4	2.37×10^{18}
150	13.9	2.46×10^{18}
200	13.5	2.52×10^{18}
250	12.3	2.76×10^{18}
300	11.4	3.00×10^{18}

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can be calculated using the Joyce–Dixon approximation[20] for a difference less than $3KT$, where K is the Boltzmann constant and T is the absolute temperature,

$$E_F = E_C + KTln\left[\frac{N}{N_C} + \frac{N}{\sqrt{8}N_C}\right], \quad (7)$$

where the temperature dependency of the effective conduction band density of states, N_C, is considered and N is the fractional ionized concentration listed in Table I. To verify the efficacy of the above method and to verify the band diagram, TCAD simulation was carried out for different temperatures with fixed doping concentrations on Ga_2O_3 and SiC to analyze the position of the Fermi level with respect to the conduction band. The simulated and experimentally extracted values are in close agreement, as shown in Fig. 10.

This confirms the band picture and suggests the possibility of a 2DEG, as indicated by the band diagram. The various band parameters derived experimentally are listed in Table II.

From the above table, the negative sign in $E_C - E_F$ suggests that the Fermi level lies above the conduction band. This was because, at 50 K, the effective conduction band density of states N_C becomes lower than the carrier concentration N. This was also verified by simulation.

Furthermore, the conduction band discontinuity can be found by considering the band diagram in Fig. 11.

From the band diagram shown above, the energy balance equation can be written as

$$\Delta E_C = V_{bi} + (E_C - E_F) + V_X, \quad (8)$$

where V_X is the energy dip in the conduction band below the fermi level on the Ga_2O_3 side, considering Eq. (8), the conduction band discontinuity is calculated and plotted for different temperatures. However, the potential dip caused by the 2DEG is not considered in the above calculation. Since both the substrate and epitaxial layer are highly doped, the capacitance was leaky, and the voltage during the C–V measurement could not be swept to a large bias due to the increase in the dissipation factor. Furthermore, the epitaxial layer is 2.7 μm, and the 2DEG formed at the heterojunction is sufficiently deep. Thus, it was improbable to measure the free carrier concentration at the heterojunction. Thus, Fig. 12 shows the conduction band discontinuity without considering the 2DEG potential.

TABLE II. Built-in potential and fermi potential for different temperatures extracted from the C–V measurement.

Temperature (K)	V_{bi} (eV)	$E_C - E_F$ (meV)
50	0.51	−4.1
100	0.46	0.2
150	0.44	7.6
200	0.43	17.3
250	0.39	26.9
300	0.37	37.2

The conduction band discontinuity is derived to be in the range of 0.4–0.5 eV without considering the 2DEG potential, which is close to the values reported.[5] However, if the 2DEG potential is determined, the exact value for the conduction band discontinuity can be determined. Another approach for determining the conduction band discontinuity is through Kromer's analysis,[32] which requires carrier profiling until the quasi-neutral region on both sides of the heterojunction. Previous reports have shown similar isotype heterojunctions formed between (Ga,In)P/GaAs,[33] InGaAs/InP,[34] and MoS_2/SiC,[30] where C–V profiling determined the conduction band and valence band discontinuities. Due to the leaky nature of the capacitance and the thick epitaxial layer, as mentioned before, we could not extract the carrier concentration to a greater depth. Thus, integrating over an incomplete carrier profile would lead to underestimating the derived values. Thus, we took the indirect approach to determine the conduction band

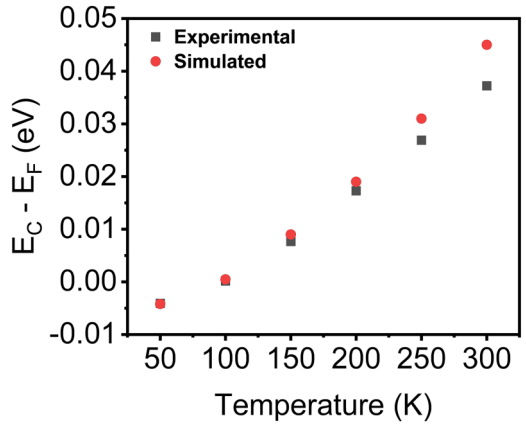

FIG. 10. Experimental and simulated result of Fermi potential with respect to the conduction band.

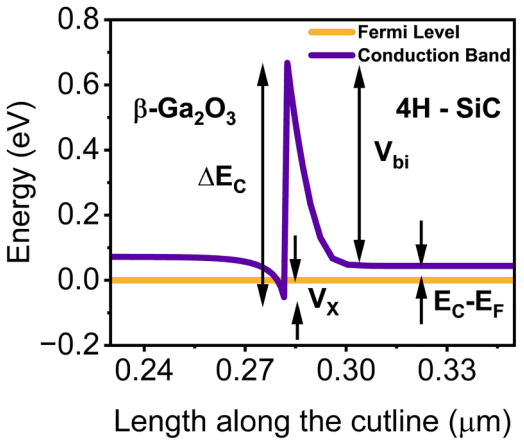

FIG. 11. Equilibrium band diagram of the heterostructure at 300 K.

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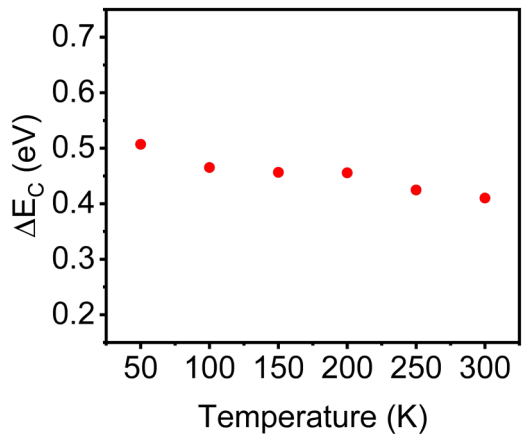

FIG. 12. Conduction band discontinuity at different temperatures.

discontinuity and indicate the possibility of the presence of 2DEG while validating the band diagram of the isotype heterojunction.

In this study, we did not consider the effect of defect states on the band discontinuity. Among the pioneering works on understanding the heterostructure band alignment, it was reported that defects and vacancies at the interface might lead to fermi-level pinning,[35] and the interface dipoles might alter the band discontinuity.[36] However, it was also found through experiment and first-order calculations that the amount of defect states does not alter the band discontinuity.[37] The interface band can trap the free carriers and result in a sheet of charge that can modulate the electric field but not the potential.[36] Thus, characterizing the interface can lead to a better understanding of the mechanism of the band lineup and the scope of future studies.

IV. CONCLUSION

In conclusion, the carrier transport in the LPCVD-grown β-Ga_2O_3/4H-SiC isotype heterojunction has been studied in this work. Both lateral and vertical devices were made in the β-Ga_2O_3/4H-SiC stack. The β-Ga_2O_3 layer was characterized by various material characterization techniques such as XRD, SEM, and AFM to confirm the quality of the grown layer. Lateral C–V measurement was employed to characterize the doping density of the top β-Ga_2O_3 epitaxial layer. Various electrical measurements were carried out to study the transport phenomenon. The suggestive band diagram echoes the possibility of the formation of 2DEG at the heterojunction on the β-Ga_2O_3 side. I–V and C–V measurements were carried out at low temperatures to validate the band diagram and show the possibility of 2DEG. Furthermore, various band parameters were extracted from the experimental result and were verified through TCAD simulation. Thus, it has been found that for the given isotype heterojunction, the TE model does not govern the transport mechanism at a lower bias and lower temperature; rather, it is attributed to a tunnelling mechanism. Furthermore, the band picture with the possibility of 2DEG has been verified through various experimental and simulation results, and the conduction band discontinuity of the heterostructure is found to be around 0.4–0.5 eV. However, characterization of the interface in terms of the defect states, interfacial dipoles, or other non-idealities might give a better understanding of the heterostructure and band lineup.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

T. Saquib: Conceptualization (equal); Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Software (equal); Visualization (equal); Writing – original draft (equal); Writing – review & editing (equal). **F. Akyol:** Conceptualization (equal); Funding acquisition (equal); Project administration (equal); Resources (equal); Supervision (equal); Validation (equal); Writing – review & editing (equal). **H. Ozden:** Data curation (equal); Formal analysis (equal); Investigation (equal); Visualization (equal); Writing – review & editing (equal). **N. Somaiah:** Data curation (equal); Formal analysis (equal); Visualization (equal); Writing – review & editing (equal). **J. Sahoo:** Formal analysis (equal); Methodology (equal); Supervision (equal); Writing – review & editing (equal). **R. Muralidharan:** Conceptualization (equal); Investigation (equal); Project administration (equal); Supervision (equal); Validation (equal); Writing – review & editing (equal). **D. N. Nath:** Conceptualization (equal); Funding acquisition (equal); Project administration (equal); Resources (equal); Supervision (equal); Validation (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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