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YILDIZ TECHNICAL UNIVERSITY
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DESIGN OF A NOVEL ASYMMETRIC TWENTY-ONE LEVEL INVERTER TOPOLOGY

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MASTER OF SCIENCE THESIS

Department of Electrical Engineering

Program of Electrical Machines and Power Electronics

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Muammer YALÇİN

Signature

Dedicated to my family

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LIST OF SYMBOLS

A	Ampere
F_{ccl}	Component Factor per Level
t_{fi}	Current Fall Time
V_d	DC Link Voltage
°	Degree
°C	Degrees Celsius
D_1	Diode 1
D_2	Diode 2
D_3	Diode 3
D_4	Diode 4
V_{dc}	Direct Current Voltage
D_f	Free-Wheeling Diode
Hz	Hertz
i	Index of the Switching Angle
V_{in}	Input Voltage
kHz	Kilohertz
Kv	Kilovolt
kVAr	Kilovolt-Ampere Reactive
kW	Kilowatt
kW/L	Kilowatts per Liter
MVA	Megavolt-Ampere
MW	Megawatt
N_{bis}	Number of Bidirectional Switches
N_{block}	Number of Blocks
N_c	Number of Capacitors
N_{dc}	Number of DC Voltage Sources
N_d	Number of Diodes
N_{gd}	Number of Gate Driver Circuits

$N_{h\text{-}bridge}$	Number of H-bridge modules
N_{level}	Number of Levels
N_{cell}	Number of Power Cells
N_{sw}	Number of Switches
N_{leg}	Number of Two-Level Inverter Legs
L_o	Output Inductance
V_{out}	Output Voltage
V_{aN}	Output Voltage Between Phase-A And Neutral Point
D_f	Overvoltage Snubber Diode
D_{t_ov}	Overvoltage Snubber Diode
C_{t_ov}	Overvoltage Snubber Capacitor
R_{t_ov}	Overvoltage Snubber Resistor
I_o	Peak Current Through the Switch During Operation
sin	Sine Function
C_d	Snubber Capacitor
α-β	Stationary Two-Axis Reference Used in Space Vector Modulation
θ_i	Switching Angle Corresponding To The i-th Level In Degrees
S	Switching Device
S_1	Switching Device 1
S_2	Switching Device 2
S_3	Switching Device 3
S_4	Switching Device 4
H_1	Switching Device 1 In H-Bridge
H_2	Switching Device 2 In H-Bridge
H_3	Switching Device 3 In H-Bridge
H_4	Switching Device 4 In H-Bridge
t	Time
TSV_{pu}	Total Standing Voltage per unit
D_{t_off}	Turn-off Snubber Diode
C_{t_off}	Turn-off Snubber Capacitor
R_{t_off}	Turn-off Snubber Resistor
D_{t_on}	Turn-on Snubber Diode
L_{t_on}	Turn-on Snubber Inductance
R_{t_on}	Turn-on Snubber Resistor
V	Volts

V_{rms}	Root Mean Square Voltage
W	Watt
α	Weighting Factors

LIST OF ABBREVIATIONS

ANPC	Active Neutral-Point-Clamped
AC	Alternating Current
BVSU	Bipolar Voltage Source Unit
CHB	Cascaded H-Bridge
CF	Cost Function
CF/L	Cost Function per Level
CSI	Current Source Inverter
DSP	Digital Signal Processor
DC	Direct Current
DFCM	Double Flying Capacitor Multicell
EV	Electric Vehicle
EMI	Electromagnetic Interference
FFT	Fast Fourier Transform
FPGA	Field Programmable Gate Array
FVSU	Fixed Voltage Source Unit
FACTS	Flexible AC Transmission Systems
FC	Flying Capacitor
GaN	Gallium Nitride
GTO	Gate Turn-Off Thyristor
HVDC	High Voltage Direct Current
LC	Inductor-Capacitor
LCL	Inductor-Capacitor-Inductor
IEEE	Institute of Electrical and Electronics Engineers
IGBT	Insulated Gate Bipolar Transistor
IGCT	Integrated Gate-Commutated Thyristor
L	Load
MBV	Maximum Blocking Voltage
MPPT	Maximum Power Point Tracking

MLDCL	Multilevel DC-Link
MLI	Multilevel Inverter
MMC	Modular Multilevel Converter
NLC	Nearest Level Control
NVC	Nearest Vector Control
NPC	Neutral-Point-Clamped
NVS	Normalized Voltage Stress
PV	Photovoltaic
PWM	Pulse Width Modulation
RSC-MLI	Reduced Switch Count Multilevel Inverter
R	Resistive
RL	Resistive-Inductive
SHE	Selective Harmonic Elimination
SHM	Selective Harmonic Mitigation
SiC	Silicon Carbide
SPWM	Sinusoidal Pulse Width Modulation
SVM	Space Vector Modulation
STATCOM	Static Synchronous Compensator
THD	Total Harmonic Distortion
TSV	Total Standing Voltage
VSC	Voltage Source Converter
VSI	Voltage Source Inverter
ZSI	Z-Source Inverter

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ABSTRACT

Design of a Novel Asymmetric Twenty-One Level Inverter Topology

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Program of Electrical Machines and Power Electronics

Master of Science Thesis

Supervisor: Assoc. Prof. Dr. Selin ÖZÇIRA ÖZKILIÇ

This research presents the design, and validation of a novel asymmetric twenty-one-level inverter topology aimed at addressing the limitations of conventional multilevel inverters (MLIs). The proposed topology is specifically developed to reduce the number of components, minimize system cost, and achieve a compact design while delivering high energy efficiency, reduced total harmonic distortion (THD), and enhanced reliability. Designed to meet the growing demand for efficient power conversion in renewable energy systems, electric vehicles (EVs), and industrial applications, the proposed inverter architecture introduces a modified MLI configuration that utilizes asymmetric DC voltage sources and an H-bridge structure to generate a twenty-one-level output voltage with high waveform quality.

To optimize harmonic performance and minimize switching losses, a Nearest Level Control (NLC)-based switching strategy is integrated, allowing for precise approximation of the reference waveform. This approach enhances overall system efficiency and reliability, with a systematic evaluation of energy performance and technical feasibility based on key performance metrics such as Total Standing Voltage (TSV) and Cost Function (CF). The proposed inverter topology has been validated through extensive simulations under various operating conditions, demonstrating robustness and adaptability. Comparative benchmarking against existing MLI designs highlights the superior performance of the proposed topology

in terms of THD reduction, improved voltage waveform quality, and cost-effectiveness.

By systematically addressing critical challenges in power electronics, this research contributes to the advancement of multilevel inverter technology. The proposed asymmetric twenty-one-level inverter topology offers a scalable, efficient, and economically viable solution that facilitates renewable energy integration, enhances system reliability, and enables significant improvements in energy efficiency.

Keywords: Multilevel inverter (MLI), asymmetrical twenty-one-level inverter, total harmonic distortion (THD), nearest level control (NLC), TSV calculation, cost function (CF).

ÖZET

Yeni Bir Asimetrik Yirmi Bir Seviyeli Evirici Topolojisi Tasarımı

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Bu araştırma, geleneksel çok seviyeli inverterlerin (MLI' ler) sınırlamalarını ele almayı amaçlayan yeni bir asimetrik yirmi bir seviyeli inverter topolojisinin tasarımını ve doğrulamasını sunmaktadır. Önerilen topoloji, bileşen sayısını azaltmak, sistem maliyetini en aza indirmek ve yüksek enerji verimliliği, düşük toplam harmonik bozulma (THD) ve gelişmiş güvenilirlik sağlarken kompakt bir tasarım elde etmek için özel olarak geliştirilmiştir. Yenilenebilir enerji sistemleri, elektrikli araçlar (EV'ler) ve endüstriyel uygulamalarda verimli güç dönüşümüne yönelik artan talebi karşılamak üzere tasarlanan önerilen inverter topolojisi, üstün dalga biçimi kalitesine sahip yirmi bir seviyeli bir çıkış voltajı üretmek için asimetrik DC kaynakları ve H-köprüsü yapılandırmasını kullanan değiştirilmiş bir MLI mimarisi sunar. Harmonik performansı optimize etmek ve anahtarlama kayıplarını en aza indirmek için En Yakın Seviye Kontrolü (NLC) tabanlı bir anahtarlama stratejisi entegre edilerek referans dalga biçiminin hassas bir şekilde yaklaştırılmasına olanak sağlanmıştır. Bu yaklaşım, genel sistem verimliliğini ve güvenilirliğini artırmakta olup Toplam Durağan Gerilim (TSV) ve Maliyet Fonksiyonu (CF) gibi temel performans parametreleri başta olmak üzere, inverterin enerji verimliliğini ve teknik fizibilitesini değerlendirmek için sistematik olarak analiz edilmektedir. Önerilen invertör topolojisi, çeşitli çalışma koşulları altında simülasyonlar yoluyla bir doğrulamaya tabi tutularak sağlamlığı ve uyarlanabilirliği gösterilmiştir. Mevcut MLI tasarımlarıyla karşılaştırmalı kıyaslama, önerilen

topolojinin THD azaltımı, iyileştirilmiş gerilim dalga şekli kalitesi ve maliyet etkinliği açısından üstün performansını vurgulamaktadır.

Güç elektroniğindeki kritik zorlukları sistematik olarak ele alan bu araştırma, çok seviyeli invertör teknolojisinin ilerlemesine katkıda bulunmaktadır. Önerilen asimetrik yirmi bir seviyeli inverter topolojisi ölçeklenebilir, verimli ve ekonomik olarak uygulanabilir bir çözüm sunarak yenilenebilir enerji entegrasyonunu, gelişmiş sistem güvenilirliğini ve önemli enerji verimliliği iyileştirmelerini kolaylaştırmaktadır.

Anahtar Kelimeler: Çok seviyeli inverter (MLI), asimetrik yirmi bir seviyeli inverter, Toplam harmonik bozulma (THD), En yakın seviye kontrolü (NLC), TSV hesabı, maliyet fonksiyonu (CF).

1
INTRODUCTION

1.1 Background and Motivation

Multilevel inverters (MLIs) have become a preferred solution in medium- and high-power applications due to their distinct advantages over traditional two-level inverters. These advantages include the generation of high-quality output voltage with reduced total harmonic distortion (THD), lower voltage stress across switching devices, and enhanced electromagnetic compatibility. Additionally, MLIs are capable of operating at lower switching frequencies while maintaining high power output, thereby improving system efficiency and reducing thermal stress on semiconductor devices. As a result, these systems not only minimize energy losses but also extend the overall lifespan of the power electronics infrastructure.

Despite their operational benefits, conventional MLI topologies face several challenges when scaled for high-voltage applications. These include an increased number of power switches, the need for numerous gate driver circuits, and reliance on multiple isolated direct current (DC) sources. Such design requirements lead to a rise in system complexity, physical footprint, and implementation cost. Particularly, as the number of voltage levels increases, the exponential growth in component count becomes a critical limitation for the practical deployment of these systems in industrial environments. This complexity also increases the burden on control strategies and modulation techniques, making real-time implementation more difficult and cost intensive.

To address these issues, recent research efforts have focused on Reduced Switch Count Multilevel Inverter (RSC-MLI) topologies, which aim to preserve the functional advantages of MLIs while minimizing component usage. By optimizing the number of switching devices and simplifying circuit design, these topologies offer a viable solution to reduce both capital cost and control complexity. Additionally, many of these RSC-MLI topologies integrate advanced modulation

schemes and innovative switching strategies that contribute to better efficiency, thermal performance, and scalability.

In recent years, a wide range of RSC-MLI configurations have been proposed, emphasizing structural innovation, modularity, and system integration. These designs are often characterized by asymmetrical source arrangements and optimized level generation techniques that allow a significant reduction in component count without compromising waveform quality. Accordingly, the development of RSC-MLIs has become a key focus area in modern power electronics, particularly for applications that demand compactness, cost-effectiveness, and high performance under stringent operating conditions.

In this context, the current research introduces a novel asymmetric twenty-one-level MLI topology that not only addresses the drawbacks of conventional MLI designs but also enhances performance across several critical parameters. The motivation for this work stems from the urgent need for power conversion systems that combine high efficiency, low THD, minimal switch count, and robust control, particularly in renewable energy, EV, and industrial drive applications. By leveraging asymmetrical DC sources, simplified H-bridge architecture, and an NLC switching strategy, the proposed topology seeks to establish a balance between performance, efficiency, and economic feasibility, thereby contributing to the evolving landscape of MLI technology.

1.2 Literature Review

The evolution of MLI topologies has significantly influenced the development of power electronic systems for medium- and high-voltage applications. The foundation of classical MLI designs was laid in 1979, when Nabae, Takahashi, and Akagi introduced the three-level Neutral-Point-Clamped (NPC) inverter, which eliminated the need for simultaneous switching of series-connected bipolar junction transistors. Their experimental setup, integrating 12 bipolar junction transistors, 12 freewheeling diodes, and six clamping diodes, successfully operated an adjustable-speed induction motor rated at 200 Volts (V) and 2.2 kilowatts (kW). This design-later commonly referred to as the NPC inverter-gained wide acceptance in industrial applications by the early 1990s.

In parallel, Baker filed a patent on a similar circuit in 1979, although it lacked experimental validation. The field continued to progress with the introduction of the three-level Flying Capacitor (FC) inverter by Meynard and Foch in 1992, which employed clamping capacitors instead of diodes. In 1994, Robicon Corporation (now part of Siemens) introduced commercial multilevel motor drives based on Cascaded H-Bridge (CHB) inverters, using modular single-phase full-bridge units to synthesize sinusoidal waveforms via Pulse Width Modulation (PWM). The modern era of MLI research was catalyzed by Marquardt's introduction of Modular Multilevel Converters (MMCs) in 2003, which rapidly found application in High Voltage Direct Current (HVDC) systems, back-to-back converters, and medium voltage drives due to their modularity, scalability, and superior output quality [1].

Over the years, numerous MLI topologies have been reported and are generally classified into two major groups based on the number of independent DC sources: single-source and multiple-source configurations. The most prominent and established topologies include the NPC, FC, and CHB inverters. FC and CHB are often referred to as multicell converters due to their modular structures comprising multiple independent power-processing units.

More recently, several advanced variations and hybrid structures have been introduced to improve specific operational features such as voltage balancing, thermal distribution, and harmonic suppression. For example, the Active Neutral-Point-Clamped (ANPC) inverter improves current-handling capacity and device reliability through better thermal stress distribution. Likewise, the Stacked Multicell topology merges serial and parallel FC cells, resulting in reduced capacitance requirements, higher output voltage levels, and enhanced waveform quality.

The Asymmetric or Hybrid CHB inverter has emerged as another innovation by employing unequal DC sources to generate a higher number of voltage levels while using fewer semiconductor switches and passive components. Similar asymmetrical concepts have also been applied to NPC-based structures, leading to enhanced performance and reduced system complexity.

These developments mark a significant shift from conventional topologies toward more compact, efficient, and scalable designs tailored for specific applications. In

light of this RSC-MLIs have attracted growing research interest as they aim to maintain the performance and waveform the quality of traditional multilevel structures while reducing the number of semiconductor switches and associated costs. RSC-MLIs represent a promising approach for the next generation of energy-efficient, cost-effective, and reliable motor drive and renewable energy conversion systems. Building upon this historical and technological foundation, the subsequent sections of this review focus on RSC-MLI topologies, which have emerged as a prominent research direction due to their potential to reduce system cost and complexity without compromising waveform quality or operational efficiency. Recent literature presents a wide range of innovative RSC-MLI configurations that aim to minimize the number of power semiconductor devices, enhance modularity, and improve overall system performance [2].

Su proposed the Multilevel DC-Link (MLDCL) inverter in 2005 as a response to the high component count in traditional MLI topologies such as NPC, FC, and CHB designs. The MLDCL topology aims to reduce the number of switches, gate drivers, and passive elements while preserving voltage waveform quality. It utilizes a cascaded half-bridge structure combined with a single-phase H-bridge inverter, forming an asymmetrical system based on discrete DC sources. Voltage synthesis is achieved through a staircase DC-link formed by half-bridge cells operating in bypass and active modes, while the H-bridge controls polarity reversal. A Digital Signal Processor (DSP)-based controller implements a duty-cycle-based switching strategy to maintain DC source utilization. Designed for low-power and high-voltage applications, the topology offers a significant reduction in switches compared to conventional designs and supports zero-voltage switching in the H-bridge. Experimental validation demonstrates high efficiency with minimal current distortion. Despite challenges in voltage balancing, especially in NPC versions, the modular and scalable nature of the half-bridge configuration positions MLDCL as a hardware-efficient solution for RSC-MLI systems [3].

Ceglia et al. (2006) proposed a simplified MLI topology, known as the T-Type inverter, to reduce the complexity and component count typical of conventional multilevel converters. The five-level inverter uses an asymmetrical H-bridge configuration with a bidirectional auxiliary switch, comprising five controlled switches, eight diodes, and two capacitors. Output voltage levels are generated

through specific switching combinations, while a built-in capacitor divider maintains voltage balance without external regulation. Modulation is achieved using a sigma-delta strategy implemented via Field-Programmable Gate Array (FPGA), allowing flexible switching frequencies and incorporating interlock delays to avoid shoot-through. Designed for medium-to-high power applications, the topology offers notable reductions in switches and diodes compared to traditional designs, along with verified efficiency and clean output waveforms. However, its dependence on FPGA control and limitations in scalability beyond five levels are noted. While modular extension is theoretically possible, it remains unvalidated experimentally. Overall, the work presents a hardware-efficient RSC-MLI topology with demonstrated performance advantages for industrial use [4].

Dixon and Moran (2006) proposed an MLI architecture based on a cascade of transistor-clamped cells, aiming to reduce switching frequency while achieving high output voltage resolution. Each cell is configured to synthesize a limited number of levels, and by cascading these blocks with varied level capacities, the structure can produce a large number of output voltage steps. The proposed system demonstrated that, for example, connecting four three-level cells in series can yield up to 81 voltage levels using only 12 transistors. The modulation strategy relies on fundamental frequency switching logic, wherein each submodule contributes proportionally to the synthesized waveform, enabling low switching losses. The architecture is modular and scalable and can be fed by either a single large DC source or multiple distributed sources, offering design flexibility. Key advantages include reduced harmonic distortion, high conversion efficiency, and ease of fault isolation due to series alternating current (AC) output connection. Despite the design's modularity, attention must be paid to ensure appropriate DC voltage distribution among modules. The topology is particularly suited for motor drives, active power filters, and EV applications requiring high-quality voltage output at low switching frequencies [5].

Ebrahim Babaei and his team proposed a new asymmetrical MLI topology designed to generate high-resolution output voltages using fewer DC sources and power switches. The structure follows a modular approach, consisting of cascaded stages connected to isolated DC sources with varying magnitudes. In each stage, a sub-inverter operates independently, and for K sources, the unit can produce multiple

output levels using only a limited number of bidirectional switches. Connecting multiple units in series exponentially increases the total number of output levels, enhanced by a voltage assignment algorithm that optimizes inter-stage interactions. DC source values follow geometric progression, improving voltage step uniformity. A fundamental frequency modulation technique, supported by a predefined lookup table, governs the switching states, reducing switching frequency and associated losses. Experimental results showed that 63 output levels were achieved with 14 switches and 6 sources, while a 343-level output was realized with 18 sources and 24 switches. The topology offers high resolution, low component count, and scalability, with low THD. However, implementation may be limited by the need for bidirectional switches and the complexity of managing isolated, non-uniform DC sources. This design is especially suitable for high-performance applications such as Dynamic Voltage Restorers, offering efficient, transformerless operation [6].

Babaei (2008) addresses the challenge of excessive switch counts in multilevel converters by proposing a cascaded submultilevel topology, known as the Cascaded Bipolar Switch inverter. The design aims to minimize switches, capacitors, and standing voltage while generating high step counts. A 53-level prototype employs 22 Insulated Gate Bipolar Transistors (IGBTs) and 6 DC sources in an asymmetrical configuration with an H-bridge for polarity reversal. Voltage synthesis is achieved through bidirectional switches in series-connected submodules, controlled via staircase modulation implemented via a microcontroller. Experimental results demonstrate a voltage THD of 3.17% and current THD of 0.23%. Limitations include bidirectional switch complexity and medium-voltage scalability constraints due to H-bridge requirements. The study contributes a modular, component-optimized solution validated through a 53-level prototype, advancing RSC-MLI efficiency in high-step applications [7].

Waltrich and Barbi (2009) introduced a three-phase cascaded MLI topology featuring power cells with two inverter legs connected in series per phase. The number of output levels per phase is defined as $2 \times N_{cell} + 1$, where N_{cell} represents the number of power cells. This series connection enables the generation of high-voltage outputs using low-voltage DC sources, contributing to enhanced modularity and scalability. A phase-shifted PWM technique is applied, effectively shifting

harmonic components to higher frequency bands and thus reducing the need for extensive filtering. Experimental validation of a three-phase prototype confirmed that the harmonic performance was comparable to traditional CHB topologies. Despite its modular benefits, the requirement for two inverter legs per cell increases the number of isolated DC sources needed, potentially complicating the system design [8].

El-Naggar and Abdelhamid (2008) introduced a novel family of MLI topologies, designed to reduce switch count compared to traditional CHB inverters while maintaining modularity and harmonic performance. The architecture is composed of a main H-bridge unit and several auxiliary switching cells, each consisting of two switches. For every added output level, only one isolated DC source and a pair of switches are required, resulting in a scalable structure that achieves $2 \times N_{dc} + 1$ levels with minimal complexity. The modulation strategy is based on Selective Harmonic Elimination (SHE) using Genetic Algorithms, which optimize switching angles to eliminate specific harmonic orders and minimize THD. Genetic Algorithm-based optimization overcomes convergence issues found in classical SHE techniques and allows operation across a wide modulation range. Experimental validation was performed using 5- and 7-level prototypes, demonstrating close agreement between simulation and hardware results. Advantages include low switching losses, extended modulation range, and reduced control effort, while a notable limitation is the high voltage stress imposed on H-bridge switches. The topology is especially appropriate for medium-power applications where harmonic compliance and switch reduction are critical [9].

Won-Kyun Choi proposed a modified H-bridge-based MLI topology that offers a simple and efficient structure capable of generating a seven-level output voltage with a reduced number of switching components. The topology consists of three independent DC sources and a total of eight switches-where the left-side switches generate intermediate voltage levels and the right-side full-bridge circuit determines the output polarity. The low component count simplifies the control algorithm; however, conventional level-based switching strategies result in high harmonic distortion, necessitating output filtering. To address this, a novel switching method incorporating PWM in the H-bridge switches was introduced. This PWM approach enables the switches to operate at the carrier frequency, producing an output

waveform that more closely resembles a sinusoid and reduces harmonic content. Based on Fourier analysis, the modulation technique is optimized to allow for output amplitude control via modulation index adjustments. Both simulation and experimental results confirm that this method yields significantly lower THD. Nonetheless, achieving the standard THD limit of 5% still requires additional filtering. Overall, the proposed topology provides a cost-effective and straightforward solution for low-power photovoltaic (PV) systems utilizing multiple DC sources, thanks to its minimal component count and simplified control [10].

Hinago and Koizumi (2010) introduced the Switched Series/Parallel Sources inverter, a single-phase multilevel topology designed to reduce switch count and enhance waveform quality, particularly for EV and renewable energy applications. The topology features an asymmetrical H-bridge configuration with discrete DC sources and uses fewer switches compared to conventional designs-requiring 11 switches for 11 levels and 14 switches for 15 levels. Voltage levels are generated by reconfiguring the DC sources in series and parallel through controlled switching, with polarity inversion handled by an H-bridge. A hybrid modulation approach combines low-frequency switching for high-voltage components with high-frequency PWM for low-voltage ones, managed via FPGA control. The inverter offers reduced harmonic distortion, fewer components, and high efficiency, making it suitable for medium- and high-power applications. Despite its advantages, the design depends on precise voltage ratios and faces challenges with bidirectional power flow. Experimental validation confirms its performance, with a THD of 14.6 percent and efficiency of 92.4 percent. The Switched Series/Parallel Sources inverter contributes a modular and hardware-efficient RSC-MLI solution optimized for practical, low-complexity power conversion needs [11].

Ouneijar et al. (2011) proposed the Packed U Cells multilevel converter to reduce the high component counts found in traditional topologies such as NPC and FC inverters. Designed as an asymmetrical structure without an H-bridge, the Packed U Cells uses fewer switches and capacitors while maintaining power quality. A seven-level version is achieved with six switches and two capacitors, using unequal capacitor voltages to generate distinct output levels through multiple switching states. A lookup-table-based PWM strategy at a fixed frequency controls voltage

balancing, ensuring reliable operation. The design is suitable for applications like motor drives and grid-connected systems due to its compactness and modular scalability. Compared to conventional converters, it achieves significant reductions in component count while maintaining performance. Despite requiring precise voltage regulation, experimental and simulation results confirm the stability and effectiveness of the topology, with a measured THD of 24.32 percent. The Packed U Cells contributes a cost-efficient and scalable solution for RSC-MLI applications, supported by hardware and simulation validation [12].

Banaei and Salary (2011) proposed a novel symmetric MLI topology aimed at minimizing the number of power switches and gate driver circuits, especially for voltage-quality improvement systems such as Dynamic Voltage Restorers. The structure comprises series-connected identical modules powered by isolated equal-magnitude DC sources, and a single H-bridge unit responsible for output polarity inversion. Each voltage level is synthesized using just two switches per module, significantly reducing conduction losses and switching path complexity. The modulation strategy is based on multi-carrier subharmonic PWM, using both the sinusoidal reference and its absolute value to determine switching states. The H-bridge operates at the fundamental frequency, toggling the polarity of the output waveform between positive and negative half-cycles. For instance, a 15-level output can be achieved using only 13 switches and 7 DC sources-representing up to 35% savings in switches and gate drivers compared to conventional symmetric CHB inverters. While this architecture ensures high efficiency and low cost of hardware, it requires careful selection of H-bridge switches due to high blocking voltage stress. Overall, the topology offers a compact, low-loss, and cost-effective solution, particularly suitable for Dynamic Voltage Restorers and voltage compensation systems [13].

Ebrahimi et al. (2012) introduced a cascaded multilevel converter topology to reduce the high component count and voltage stress present in traditional MLI designs. The proposed asymmetrical structure employs multilevel modules with unequal DC sources and bidirectional switches to generate multiple voltage levels, while full-bridge units manage polarity inversion. Voltage levels are synthesized by activating one switch per module in coordination with the full bridge to avoid short circuits. A fundamental frequency switching strategy approximates the

reference waveform without harmonic optimization. Designed for high-power quality applications using distributed DC sources, such as PV or fuel cell systems, the topology reduces the number of switches, diodes, and gate drivers. It also offers modular scalability and improved efficiency. A prototype generating 125 output levels with 24 switches and a peak voltage of 400 volts achieved a THD of 5.9 percent. Despite requiring multiple isolated sources and subjecting switches to high blocking voltages at elevated levels, the design provides a validated and efficient solution for RSC-MLI applications [14].

Najafi and Yatim (2012) proposed the Reversing Voltage MLI to address component count, control complexity, and voltage balancing issues in conventional inverter designs. The symmetrical topology utilizes equal DC sources and separates high-frequency level generation from low-frequency polarity reversal using a full-bridge. The high-frequency stage produces unipolar voltage levels, while the H-bridge operates at line frequency to generate bipolar output. The design uses fewer semiconductor switches, gate drivers, and isolated sources than traditional topologies. A phase-disposition PWM strategy further reduces control complexity by halving the number of carrier signals. A seven-level configuration is achieved with 10 switches and 3 sources, offering lower conduction losses and high modularity. The Reversing Voltage inverter is suited for high-voltage applications such as HVDC systems, flexible AC transmission systems (FACTS), and renewable energy. Experimental validation confirms THD of 3.85 percent and high efficiency, though the structure depends on isolated DC sources and lacks internal voltage-balancing mechanisms. Compared to conventional topologies, the Reversing Voltage inverter requires fewer components and achieves compliance with harmonic standards, making it a compact and cost-effective RSC-MLI alternative for power-critical systems [15].

Nilkar, Babaei, and Sabahi (2012) proposed a cascaded MLI topology that reduces switch count while maintaining high voltage resolution by using four-level basic cells. The design features an asymmetrical H-bridge structure formed by connecting two four-level cells in series, each with two DC sources and four switches, along with an H-bridge for polarity inversion. A 21-level output is achieved using only 12 switches, offering a 40 percent reduction compared to conventional CHB designs. Voltage levels are generated through specific switching states that enable

source connection, series combination, bypass, or zero output. The modulation uses fundamental frequency staircase control to minimize switching losses. Targeted at renewable energy systems, the topology supports binary or unary source scaling, allowing modular expansion up to 31 levels. Although the use of asymmetric DC sources may complicate implementation, the design improves switch utilization and reduces source variation. Simulations confirm 21 output levels with 1.0 percent THD under resistive-inductive (RL) loading. The work provides a scalable and hardware-efficient RSC-MLI solution validated through modular cell cascading and low-frequency control [16].

Kangarlu and Babaei introduced a generalized cascaded MLI topology, termed the Two Switched Enable Generation inverter, to enhance waveform quality while reducing the number of switching devices in high-power systems. The design employs modular subunits with multiple DC sources and switches, followed by an H-bridge for polarity inversion. It operates in either symmetrical or asymmetrical mode, synthesizing voltage levels through coordinated control of bidirectional and unidirectional switches. A staircase modulation strategy ensures low switching frequency and reduced losses. Compared to conventional CHB designs, the Two Switched Enable Generation topology lowers switch count and gate driver requirements while achieving improved efficiency and modularity. Despite increased voltage stress on H-bridge switches, experimental results confirm low THD and effective performance under inductive loads, affirming its suitability for industrial and renewable energy applications [17].

Babaei et al. (2013) proposed an asymmetrical cascaded MLI topology aimed at minimizing the number of switches and driver circuits while maximizing the number of output levels. Each basic unit is composed of six unidirectional switches and two isolated DC sources, producing up to seven levels individually. By cascading two such units, the topology achieves 49 output voltage levels using only 12 switches and five DC sources. A look-up table-based control strategy with fundamental frequency switching is employed. Simulation and experimental results confirm high-resolution output with THD values of 4.1% for voltage and 3.1% for current. While the structure ensures hardware efficiency and scalability, the use of asymmetrical DC source ratios adds complexity to implementation [18].

Gautam et al. (2013) introduced an asymmetrical MLI topology using a trinary sequence of DC sources to minimize switch count while maximizing output voltage resolution. For a total of N_{dc} (number of DC voltage sources), the proposed structure can generate up to three times N_{dc} output voltage levels by utilizing only four times N_{dc} plus one power electronic switches. Output voltages are synthesized using algebraic combinations of DC source voltages. A 100 Hertz (Hz) multi-carrier PWM modulation scheme is implemented, using a 50 Hz sinusoidal reference for carrier comparison. Complementary switching pairs handle opposite half cycles. Simulation of 9- and 27-level configurations showed voltage THD values of 6.2% and 2.68%, respectively, and current THD as low as 0.92%, confirming high-resolution, low-component operation. Nonetheless, the method requires precise control of source magnitudes and complex mapping algorithms [19].

Toupchi Khosroshahi introduced the Crisscrossed Cascade MLI topology to reduce the component count, conduction losses, and complexity associated with traditional CHB converters. Designed for medium-voltage applications, the topology employs asymmetrical H-bridge modules with bidirectional switches, enabling both symmetric and asymmetric configurations. Voltage levels are generated through modular units combining DC sources, with polarity reversal handled by an H-bridge. A phase-shifted SPWM technique, implemented via digital controllers and gate drivers, governs the switching strategy. The Crisscrossed Cascade inverter achieves significant reductions in switch count and peak inverse voltage, offering improved harmonic performance and scalability. Experimental validation confirmed low THD and efficient operation for 13- and 31-level outputs, though reliance on multiple DC sources and binary scaling adds control complexity [20].

Babaei et al. introduced the Hexagonal Switched Cell MLI to reduce component count and enhance modularity in high-voltage systems. The topology consists of cascaded asymmetrical H-bridge modules using unidirectional switches and isolated DC sources, producing multiple voltage levels through complementary switching without leg overlap. Designed for applications such as renewable energy integration and motor drives, the Hexagonal Switched Cell inverter offers reduced switch count, lower voltage stress, and scalable structure. A 49-level prototype demonstrated improved efficiency with significant IGBT savings and minimal current distortion under inductive loading. Despite reliance on isolated DC sources

and asymmetric scaling, the architecture presents a cost-effective and experimentally validated solution for high-power applications [21].

Gupta and Jain introduced the Cross Connected Sources MLI to reduce the switch count and complexity found in conventional high-level MLI topologies. By utilizing alternately polarized floating DC sources and eliminating the H-bridge, the topology achieves additive voltage synthesis with fewer components. A five-level configuration operates through eight switching modes controlled by a multicarrier PWM scheme, enabling efficient voltage generation with reduced switching losses. Experimental validation confirmed stable operation and acceptable harmonic performance under inductive loads. Despite reliance on isolated sources and limited fault tolerance, the Cross Connected Sources design offers significant reductions in components and losses, making it suitable for renewable energy systems, EVs, and medium-voltage drives [22].

Mokhberdoran and Ajami proposed a modular cascaded MLI designed to reduce switch count and circuit complexity while achieving high voltage resolution. The topology comprises basic blocks with six IGBTs and two DC sources, forming an asymmetrical, H-bridge-free structure. Output voltage levels are synthesized through series-connected modules, with symmetric configurations generating linear level progression and asymmetric modes enabling exponential scaling via binary, geometric, or septenary DC source arrangements. A multicarrier PWM scheme manages switching, distributing thermal stress across blocks. Experimental validation confirmed scalable operation up to 49 levels, with reduced THD and 25-50% fewer switches than conventional CHB inverters. Despite higher voltage stress and reliance on isolated sources, the design demonstrates efficiency, modularity, and suitability for industrial and grid-tied systems [23].

Babaei et al. introduced a cascaded MLI topology aimed at reducing IGBT count, driver circuits, and DC sources in medium-voltage high-power systems. The design employs asymmetrical DC sources and unidirectional switches arranged in modular H-bridge structures. Voltage levels are generated through additive or subtractive combinations of sources, controlled by a fundamental frequency switching strategy that minimizes switching losses. A 31-level prototype demonstrated high efficiency and low THD under inductive loading. The topology offers scalability and reduced voltage stress compared to conventional designs, though it requires varied DC

source magnitudes, increasing control complexity. This work contributes a cost-effective, experimentally validated architecture to RSC-MLI research [24].

Gupta and Jain (2014) proposed a cascaded MLI topology, termed Switched DC Sources, to reduce the number of power switches while maintaining waveform quality in high-power systems. The design eliminates H-bridges by using complementary switching of symmetrical isolated DC sources and unidirectional-blocking switches for voltage synthesis across eight modes. A multicarrier PWM with alternate phase opposition disposition controls high-voltage switches at 50 Hz and low-voltage switches at 1 Kilohertz (kHz) to balance losses. The topology is applicable to renewable energy systems, EVs, and medium-voltage drives, offering fewer switches and lower switching losses than CHB inverters. However, it requires isolated sources, exhibits limited fault tolerance, and involves higher-rated inner switches. A five-level prototype achieved 36.89% simulated voltage THD, confirming the topology's feasibility and efficiency [25].

Mohamad Reza Banaei and his collaborators proposed a semi-cascaded MLI topology that enables high-level output generation using a minimal number of switches, offering operational flexibility with both symmetric and asymmetric DC sources. The topology is constructed by appropriately connecting identical cells, each consisting of one DC source and two switches. The complete structure achieves both positive and negative output polarities using only six switches. In the symmetric configuration, all DC sources are equal, resulting in 2 x N_{dc} +1 output levels. In contrast, the asymmetric configuration employs geometrically scaled DC sources, significantly increasing the number of output levels. Output voltage is synthesized through selective switching paths determined by a control algorithm, which defines the conduction states for each level. A fundamental frequency-based fixed switching strategy is used, where predefined lookup tables assign switching states to corresponding voltage levels. Compared to conventional cascaded and semi-cascaded topologies, this design reduces the number of switching components, lowers total peak inverse voltage, and minimizes switching losses due to fewer active switches. However, in the asymmetric case, maintaining precise voltage ratios between sources presents a practical limitation. Overall, Banaei's topology offers a compact, cost-effective, and modular solution, particularly well-suited for medium-voltage applications [26].

Babaei, Laali, and Bayat (2015) presented a cascaded MLI structure using positive-level-producing basic units. Each unit contains three isolated DC sources and five unidirectional switches, enabling three output levels. Cascading multiple such units along with an H-bridge generates full-wave AC output. A fundamental frequency modulation strategy governs switching, using a pre-programmed Erasable Programmable Read-Only Memory lookup table controlled by a microcontroller. The experimental 15-level prototype demonstrates low THD and efficient output generation using just 12 switches. The architecture is cost-effective and compact but relies on the availability of multiple isolated and unequal DC sources, which may limit its practical deployment [27].

Babaei, Laali, and Bahravar (2015) developed a modular cascaded MLI structure composed of basic units, each integrating two DC sources and one H-bridge. The topology supports both symmetrical and asymmetrical configurations and allows generation of multiple output levels using five proposed source algorithms. The most effective algorithm minimizes component count and blocking voltage. The sub-symmetric version incorporates full- and half-wave charge balance control. Both fundamental frequency and PWM control techniques are applicable. An experimental 81-level prototype validates its modularity, efficiency, and practical viability for high-resolution inverter applications with reduced switching losses and system cost [28].

Babaei and Laali (2015) proposed an optimized cascaded MLI topology using basic units built exclusively from single-directional switches and multiple DC sources per leg. Each unit consists of a specific number of power switches, with DC source voltages determined by two alternative algorithms: fixed-ratio scaling and cumulative incremental logic. Architecture enables both positive and negative level generation with high output resolution. Modulation is based on fundamental frequency switching, selecting the DC level closest to the sinusoidal reference. Benefits include reduced blocking voltage, low component count, and scalable design. However, complexity in source configuration and control remains a limiting factor for practical applications [29].

Reza Barzegarkhoo et al. proposed a Switched-Capacitor MLI topology designed to generate high resolution output voltage levels using a reduced number of switches. The design is based on a novel switched-capacitor converter module that

utilizes series-parallel transformation to boost input voltage and create multiple virtual DC levels. Each switched-capacitor converter unit includes one isolated DC source, one capacitor, one diode, and two switches, with capacitor voltages regulated by a binary asymmetric self-balancing algorithm, eliminating the need for external balancing circuits. A low-switch-count polarity reversal unit replaces the conventional H-bridge, minimizing conduction paths and component count. The topology supports both symmetrical and asymmetrical sources, with improved performance under asymmetrical conditions. For example, it achieves 49 levels with 14 switches and 3 sources, and 137 levels with 18 switches and 4 sources. Controlled by fundamental frequency modulation and logic-based switching, it ensures low switching losses and stable capacitor voltages. Key benefits include high output resolution, low component count, low voltage stress, high efficiency, and modularity, while its main limitation is the need for isolated sources per switched-capacitor converter unit. This structure presents a compact, scalable, and cost-effective solution for renewable energy and distributed generation systems [30].

Samadaei et al. (2016) proposed an asymmetrical MLI topology featuring an Envelope Type module to reduce switch count and voltage stress in high-power systems. The design eliminates H-bridge usage by using bidirectional switches and diode-blocking paths to synthesize bipolar voltage levels from four asymmetric DC sources, achieving 13 output levels with 10 switches. SHE PWM with six angles per quarter-cycle is applied at 50 Hz, reducing 3rd to 19th harmonics and achieving 3.46% simulated THD. The topology offers modular scalability, inherent bipolar output, and 96.56% efficiency under resistive (R) load, requiring fewer switches and sources than conventional MLIs. Compared to NPC, CHB, and U-cell configurations, it reduces TSV and improves component efficiency. Experimental results using ATMEGA16-controlled IGBTs confirm 4.54% THD under RL load, meeting Institute of Electrical and Electronics Engineers (IEEE) 519 standards without filtering. Despite requiring asymmetric DC sources, the design presents a scalable and hardware-efficient RSC-MLI solution for HVDC and renewable energy systems [31].

Samadaei et al. (2017) introduced the Square T-type module to enhance RSC-MLI performance by generating high-level output voltages with fewer switches and

simplified circuitry. Designed without a traditional H-bridge, the asymmetrical structure consists of 12 switches and four unequal DC sources, producing 17 voltage levels through two T-type cells arranged in a square configuration. This configuration inherently generates output polarity without requiring any auxiliary circuitry. The topology uses Nearest Level Control (NLC) for efficient modulation with low computational demand. Aimed at large-scale PV systems, it offers reduced THD, compact design, and modular scalability. Its main limitation is the complexity of managing asymmetrical sources. Compared to CHB and conventional T-type inverters, the Square T-Type achieves higher output levels with fewer components and a simpler structure. Simulation and experimental validation confirm its practicality and effectiveness in advancing scalable, efficient RSC-MLI solutions [32].

Prabaharan et al. (2020) proposed a trinary sequence-based MLI topology to achieve high output voltage levels with minimal components. Using a 1:3 asymmetrical DC source ratio, the design generates nine output levels with only nine switches and two isolated sources. The topology includes a level generation unit and an H-bridge polarity reversal unit, structured to avoid short circuits through non-overlapping switch activation. A unipolar phase-disposition PWM reduces carrier requirements, with high-frequency switching for level generation and fundamental frequency for polarity reversal. Aimed at renewable energy systems, FACTS devices, and medium-voltage drives, it offers 50% fewer switches than conventional CHB topologies and supports modular scalability. Limitations include reliance on isolated sources and high voltage stress on H-bridge switches, addressed using integrated gate-commutated thyristors (IGCTs). Simulation and experimental results confirm the effectiveness of the design in delivering 240 V output with balanced efficiency and waveform quality, advancing compact and efficient RSC-MLI architectures [33].

In this section, a systematic review of the key contributions in the field of RSC-MLI topologies has been conducted in line with the historical and technological context previously outlined. Each study has been evaluated in terms of its design motivations, proposed topology and operating principles, employed modulation or control strategies, targeted application domains, reported advantages and limitations, and specific contributions to literature. This comprehensive analysis

provides deeper insight into current research trends and highlights the potential of RSC-MLI configurations as viable alternatives to conventional MLI structures. Most of the reviewed topologies introduce noteworthy innovations aimed at optimizing switch count, enhancing modularity, and preserving waveform quality. These findings clearly underscore the growing relevance and applicability of RSC-MLIs in modern power electronic systems.

1.3 Objectives of the Study

The primary objective of this study is to design and analyze a novel asymmetric twenty-one-level MLI topology that addresses the inherent limitations of conventional inverter architectures in terms of component count, harmonic distortion, and structural complexity. The study specifically aims to minimize the number of active power switches and DC voltage sources, thereby reducing system cost, control complexity, and physical volume, without compromising output waveform quality.

To this end, the proposed topology employs asymmetrically scaled DC sources in conjunction with an H-bridge-based architecture to generate twenty-one discrete output voltage levels. The system is further enhanced through the application of an NLC switching strategy, which operates at the fundamental frequency to reduce THD and switching losses while maintaining close tracking of a sinusoidal reference waveform.

The study also aims to evaluate the proposed inverter's performance through key technical indicators such as Total Standing Voltage (TSV), Cost Function (CF), and Component Factor per Level (F_{ccl}). Simulation-based analyses are conducted under both R and RL load conditions to assess the inverter's capability in producing high-quality stepped output waveforms compliant with IEEE harmonic standards. Finally, a comparative benchmarking is performed against existing RSC-MLI topologies to demonstrate the advantages of the proposed system in terms of harmonic suppression and cost-efficiency.

By systematically addressing major challenges in the field of power electronics, this research seeks to contribute to a scalable, compact, and energy-efficient solution suitable for integration in renewable energy systems, EV drives, and industrial power conversion applications.

1.4 Scope and Limitations

This study focuses on the design and simulation-based evaluation of a novel asymmetric twenty-one-level MLI topology intended for medium- and high-power applications, including renewable energy systems, EV drives, and industrial motor control. The scope encompasses the development of an RSC-MLI architecture that utilizes asymmetrical DC voltage sources in combination with an H-bridge-based configuration. This structural approach is designed to generate a high-resolution stepped output waveform while minimizing the number of active power switches and overall component usage. The inverter employs an NLC modulation strategy, which operates at fundamental switching frequency to enhance harmonic performance, reduce switching losses, and improve overall system efficiency.

Key performance metrics-including THD, TSV, CF, and F_{ccl} - are evaluated through detailed simulation-based analysis under different load conditions (R and RL). Comparative benchmarking against conventional MLI topologies is conducted to demonstrate the advantages of the proposed system in terms of harmonic suppression, waveform quality, and cost-effectiveness. The study particularly emphasizes the inverter's potential for scalability, compactness, and suitability in thermally constrained environments.

However, the study is subject to several limitations. Firstly, all validation procedures are confined to simulation environments; no experimental hardware prototype was developed or tested. As such, real-world non-idealities, including parasitic effects, switching delays, and thermal variations-were not accounted for. Secondly, the analysis assumes ideal switching behavior and static load conditions, which may diverge from dynamic scenarios encountered in practical applications such as motor drives or grid-tied inverters. Thirdly, while the NLC modulation is effective for high-level voltage synthesis, its behavior under control signal delays and frequency drift are not investigated. Lastly, critical design aspects such as electromagnetic interference (EMI), long-term thermal reliability, fault tolerance, and protection mechanisms fall outside the scope of this research.

Despite these limitations, the study provides a meaningful conceptual and technical contribution by introducing a structurally compact and cost-efficient MLI solution capable of generating high-fidelity output waveforms using a reduced number of

components. The findings form a solid basis for future research and hardware-level development toward practical implementation in advanced power electronics systems.

1.5 Thesis Organization

This thesis is systematically structured into eight main chapters to present the design, analytical modeling, and performance evaluation of a novel asymmetric twenty-one-level inverter topology. Each chapter is methodically organized to contribute progressively to the reader's understanding of the proposed system and its technical merits.

- Chapter 1 provides an introduction to the research problem, outlines the motivation and background, and clearly states the objectives of the study. An extensive literature review is conducted to identify research gaps, leading to the definition of the original contributions. The chapter also presents the scope, limitations, and an overview of the thesis structure.
- Chapter 2 explains the fundamental principles of inverter operation and highlights their significance in power electronics. It introduces a general classification of inverters, Current Source Inverters (CSIs), Voltage Source Inverters (VSIs), and Z-Source Inverters (ZSIs)-and elaborates on their operational characteristics. The chapter further analyzes the evolution from two-level inverters to MLI systems, emphasizing technical motivations for this transition.
- Chapter 3 presents a technical evaluation of established MLI topologies including NPC, FC, CHB, ANPC, MMC, and RSC-MLI configurations. The chapter discusses modulation techniques such as SHE, SVPWM, and Phase-Shifted PWM, and summarizes MLI applications in renewable energy systems, EVs, HVDC transmission, and industrial drives. It concludes with a synthesis of identified research gaps that form the basis for the proposed work.
- Chapter 4 describes the conceptual and technical details of the proposed topology. It introduces the novel circuit configuration, the asymmetrical voltage source assignment, and the NLC modulation approach used for voltage level synthesis. The chapter also highlights key design advantages

including reduced switch count, improved waveform quality, and structural simplicity.

- Chapter 5 outlines the methodology used to model the proposed topology through analytical derivations and parametric evaluation. In addition to employing simulation tools such as PSIM and MATLAB/SIMULINK, this study incorporates hand-derived formulations and structured scenario-based analyses under both R and RL load conditions. Performance metrics such as THD, TSV, CF, and F_{ccl} are comprehensively evaluated. Benchmark comparisons with conventional and RSC-MLI topologies from the literature are also included.
- Chapter 6 presents the performance analysis based on the analytical framework. Harmonic content, switching behavior, and waveform quality are examined in detail, and the results are benchmarked against comparable inverter structures from literature. The discussion further explores the practical implications of the proposed topology in terms of cost-effectiveness, component optimization, and potential use cases.
- Chapter 7 provides a summary of the study's findings and key technical contributions. The limitations of the current work are addressed, and directions for future research, including experimental validation, dynamic loading, and real-time control implementation are suggested.

At the end of the thesis, references, appendices, and scientific publications derived from this research are provided. The structured and progressive format of the thesis facilitates a clear understanding of both theoretical development and the technical relevance of the proposed inverter topology.

2
INVERTER TECHNOLOGY: PRINCIPLES, CLASSIFICATIONS, AND TOPOLOGICAL PROGRESSION

This chapter presents a comprehensive overview of inverter technology, encompassing its fundamental operational principles, functional significance in power electronics, and evolving topological structures. It begins by outlining the core mechanisms through which inverters perform DC to AC conversion, emphasizing the role of switching techniques and modulation strategies. The discussion proceeds with a general classification of inverters, distinguishing between CSIs, VSIs, and the more recent ZSIs, each offering unique characteristics and application scopes.

The chapter then focuses on VSIs, delving into their internal classification into two-level and multilevel structures. It elaborates on the architectural and functional differences, particularly highlighting the limitations of traditional two-level inverters in producing high-quality output voltages. This naturally leads to the introduction of MLIs, which provide enhanced voltage resolution and reduced harmonic content. Finally, the chapter addresses the need for advanced inverter topologies to meet the growing demand for high-performance and energy-efficient power conversion in modern applications.

2.1 Fundamentals of Inverter Operation

Inverters are fundamental components in modern power electronics, responsible for converting DC into AC, thus playing a vital role in a wide range of industrial, commercial, and renewable energy systems. To fully comprehend their functionality and integration within power systems, it is essential to first understand their operational fundamentals. Accordingly, this section will address two key subtopics: the basic operating principles of inverters and their importance in the field of power electronics.

2.1.1 Basic Operating Principles of Inverters

Inverters are power electronic devices that convert DC into AC. Their primary function is to transform the DC power supplied by sources such as batteries or PV

systems into usable AC with desired voltage magnitude, frequency, and phase. This transformation is achieved through switching control strategies, commonly implemented using PWM techniques [34].

To effectively convert DC into AC, inverters are employed using specific switching strategies that define their operation and output waveform characteristics. The fundamental working principles of inverter circuits can be understood by examining basic topologies such as the half-bridge and full-bridge inverters. These configurations serve as the foundation for more advanced multilevel and modular inverter systems. The following sections present a detailed overview of their structure, switching mechanisms, and output behavior, providing a basis for understanding inverter functionality under various load conditions.

Inverters can be classified in various ways based on the type of power supply (VSIs, CSIs etc.), number of output phases (single-phase, three-phase), control strategy applied (square wave, modified square wave, or PWM inverters), and isolation characteristics (isolated or non-isolated). In addition, inverters can also be categorized according to their circuit topology. In this study, the focus will be solely on single-phase inverters, and their classification will be based on their circuit configurations. Specifically, the analysis will be structured in the following order: half-bridge inverters, full-bridge inverters, and push-pull inverters. Each topology will be explained in detail in the subsequent sections [35].

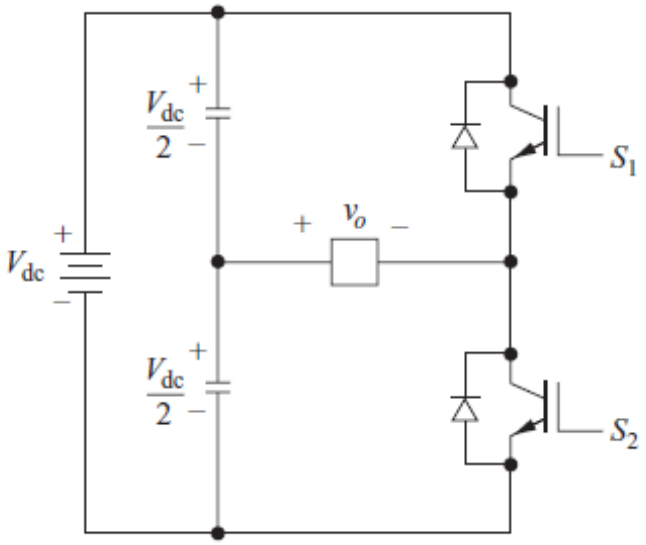


Figure 2.1 Single-phase half-bridge inverter [34]

The half-bridge inverter configuration, as illustrated in Figure 2.1, serves as a fundamental topology for DC to AC conversion. This circuit, initially introduced in Chapter 2 for use in DC power supply systems, employs only two power switches. The reduction in switch count is achieved by dividing the DC input voltage into two equal halves using a pair of capacitors of identical value, each charged to $V_{dc}/2$.

When switch S_1 is activated, the load experiences an output voltage of $-V_{dc}/2$, whereas closing switch S_2 results in $+V_{dc}/2$ at the load terminals. This operation allows the generation of a two-level square waveform, or a bipolar PWM output.

It is important to note that each switch, when turned off, must withstand the entire DC bus voltage V_{dc}, which is double the load voltage. Like the full-bridge inverter, a dead time between switching events is necessary to avoid short-circuiting the DC supply. Additionally, freewheeling diodes are incorporated across the switches to ensure continuous current flow, particularly when driving inductive loads.

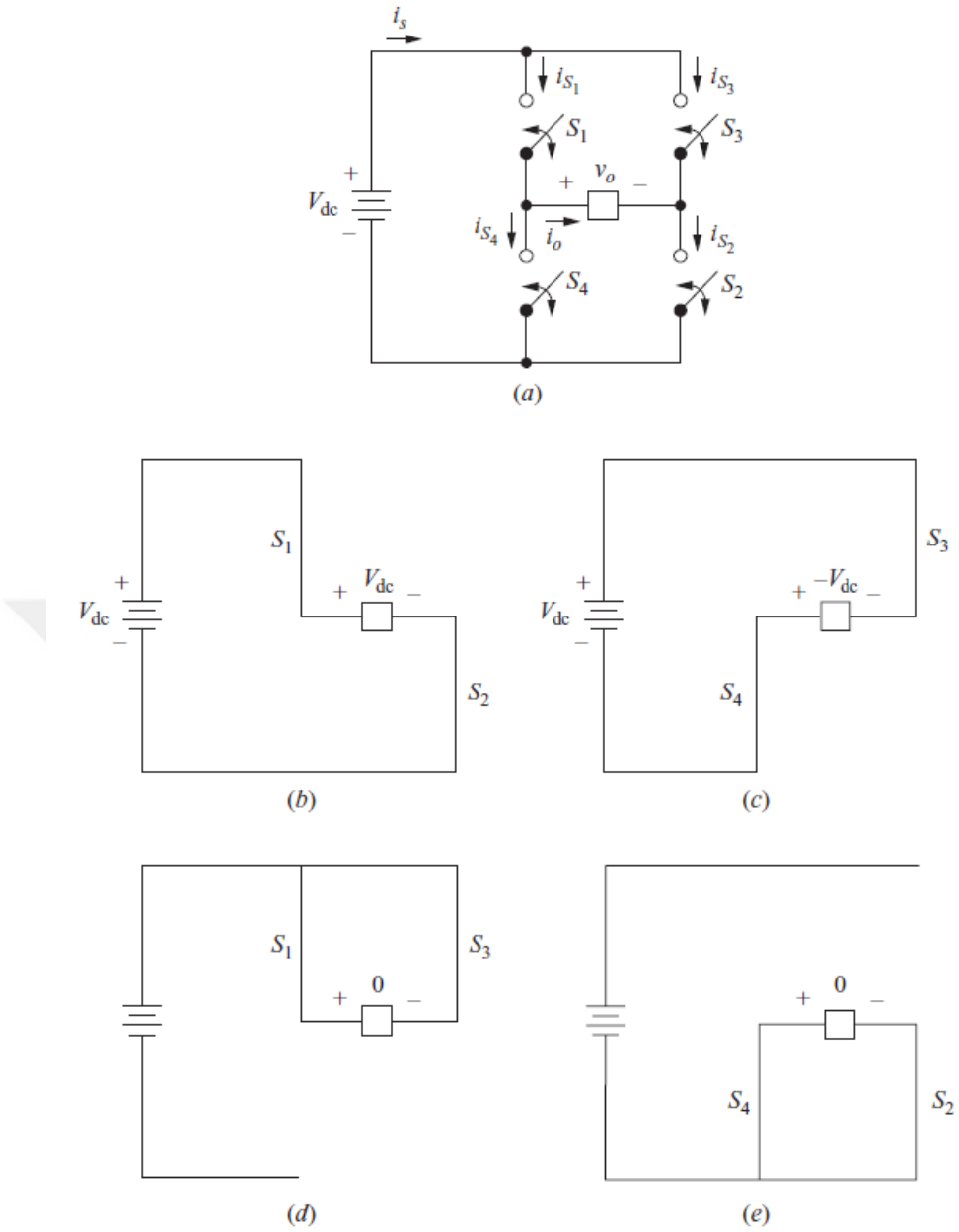


Figure 2.2 (a) Full-bridge inverter topology; (b) switches S_1 and S_2 are turned on; (c) switches S_3 and S_4 are turned on; (d) switches S_1 and S_3 are conducting; (e) switches S_2 and S_4 are conducting [34]

The full-bridge converter, as depicted in Figure 2.2a, represents a fundamental topology for converting DC input into AC output. Previously introduced in Chapter 2 as part of a DC power supply architecture, this converter synthesizes an alternating output voltage by appropriately controlling the switching sequence of its power switches. Depending on which switches are activated, the output voltage v_o can assume values of $+V_{dc}$, $-V_{dc}$, or zero. Figures 2.2b to 2.2e illustrate the corresponding equivalent circuits for different switch combinations.

It is critical to ensure that switches S_1 and S_4, or S_2 and S_3, are never turned on simultaneously, as this would result in a direct short circuit across the DC supply. To prevent such occurrences, adequate switching intervals- referred to as blanking time- must be incorporated in the control strategy. Failure to maintain this timing can lead to shoot-through faults, where both switches in a leg conduct simultaneously, potentially damaging the power circuit.

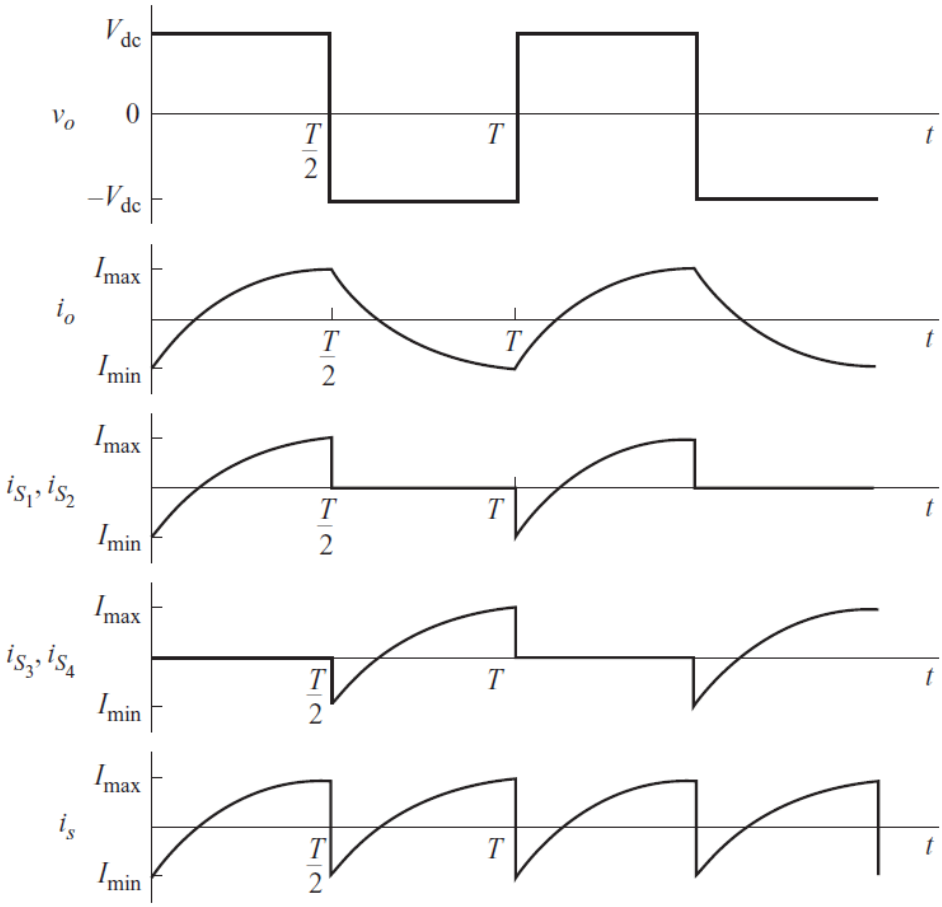


Figure 2.3 Outputs of the full-bridge inverter topology with RL load [34]

The full-bridge inverter topology is widely employed in power electronic systems for generating an AC output from DC input. As illustrated in Figure 2.3, the output voltage waveform consists of alternating square pulses, which are typically applied across various load types such as resistive, inductive, or RL combinations. In the case of an RL load, the voltage waveform maintains its square-wave nature; however, the current waveform exhibits a delayed and smoother response due to the energy storage characteristics of the inductor. This phase lag between voltage and current becomes more pronounced as the inductive reactance increases. The

figure clearly demonstrates the steady-state behavior of the inverter, emphasizing the influence of load impedance on waveform shape and timing [34].

Among various inverter topologies, the classical push-pull inverter is well-known for its structural simplicity and robustness, making it a widely adopted solution in single-phase Uninterruptible Power Supply systems. It operates based on the alternate switching of two semiconductor devices; each connected to opposite ends of the center-tapped transformer primary. During operation, each switch conducts alternately to apply positive or negative voltage pulses to the transformer, thereby generating a bipolar rectangular waveform at the secondary. However, when used with inductive loads, the root-mean-square output voltage tends to vary significantly with the load current, making duty cycle modulation ineffective for consistent voltage control. Moreover, in ferro resonant-based systems, where no modulation is typically employed, the voltage waveform applied to the transformer primary contains high harmonic content, particularly the third harmonic. This results in increased reactive power circulation through both the switching devices and the transformer, leading to reduced system efficiency and bulkier magnetic components. Despite these limitations, the two-level push-pull inverter remains a relevant reference architecture due to its foundational role in the development of multilevel variants and its straightforward implementation in low- to medium-power applications.

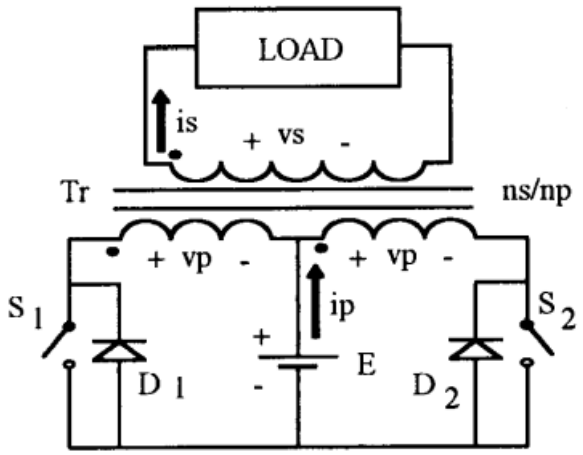


Figure 2.4 Push-pull inverter topology [36]

Figure 2.4 illustrates the classical push-pull inverter topology, comprising two active switches (S_1 and S_2) connected to a center-tapped transformer primary. Each

switch operates in an alternating manner, allowing current to flow through one half of the transformer winding during its conduction period. This action produces a bipolar rectangular voltage waveform at the transformer's secondary, essential for AC generation. The figure also highlights the presence of freewheeling diodes connected across each switch to support the continuity of inductive load current during switching transitions. This configuration ensures the basic functionality of the inverter, albeit with limitations in harmonic suppression and voltage regulation under varying load conditions. The symmetric switching sequence results in a two-level output waveform, making it less effective in applications where high-quality sinusoidal output is required without extensive filtering [36].

Understanding the basic operating principles and switching behaviors of inverter topologies such as the half-bridge and full bridge forms the cornerstone for analyzing more complex inverter systems. These fundamental architectures not only demonstrate how DC can be effectively transformed into AC through precise switch control but also provide insight into essential design considerations such as voltage stress, switching delays, and current continuity. Building upon this foundational knowledge, it is now pertinent to explore the broader role that inverters play within the field of power electronics. Their significance extends far beyond basic conversion tasks, contributing critically to energy efficiency, grid integration, and the control of modern electric drives and renewable energy systems. The following section discusses the multifaceted importance of inverters in contemporary power electronic applications.

2.1.2 Importance of Inverters in Power Electronics

Modern power systems are undergoing a transformation from centralized to distributed generation architecture. As renewable energy sources such as wind, solar, and fuel cells become more prevalent, the role of inverters in facilitating grid integration has become increasingly vital. Inverters not only perform energy conversion but also manage active/reactive power flow, voltage and frequency regulation, and harmonic mitigation, thereby enhancing system stability and efficiency [37].

In large-scale installations such as offshore wind farms, inverters enable real-time power control and high-performance grid interfacing. MLI topologies are especially

valued in such contexts for their modularity, fault tolerance, and energy efficiency, marking them as essential technologies for the future of power electronics [37], [38].

In the context of PV systems, major manufacturers like ABB, Siemens, SMA, Danfoss, and Mitsubishi have significantly advanced inverter topologies to meet rising performance, efficiency, and safety standards. ABB's PVS300, built on a three-level NPC topology, offers high power density and transformerless operation tailored for commercial and residential rooftop applications. Siemens has commercialized module-integrated microinverters optimized for compactness and modular deployment [39].

In the context of medium-voltage industrial applications, inverters-especially MLIs - are indispensable for achieving high performance, improved power quality, and energy efficiency. Although less than 5% of medium-voltage motors currently operate under variable speed drives, there is vast potential for energy savings by adopting MLI-based systems. Variable-speed operation not only reduces energy losses but also allows process optimization and enhanced dynamic response in critical industrial sectors such as oil and gas, water treatment, chemical processing, and mining.

Several major industrial players have commercialized advanced MLI-based drive systems. ABB, for instance, utilizes the three level NPC configuration in its ACS2000 medium-voltage drive series, which emphasizes compactness, transformerless operation, and high-power quality. The drives are capable of regenerative breaking and maintain sinusoidal input currents with unity power factor, fulfilling stringent grid code requirements. Similarly, Siemens has adopted this topology in its SINAMICS Perfect Harmony drives, offering a scalable solution with high reliability and minimal filter requirements. These systems are particularly effective in applications such as centrifugal compressors, pumps, and marine propulsion, where robust control and low distortion are paramount [40].

In addition to classic MLIs, SMA introduced advanced H5 inverter topology for string inverters, which eliminates freewheeling current loss and minimizes leakage currents in transformerless systems. Sunways developed the HERIC architecture that separates the grid filter from the converter during freewheeling for improved

efficiency. Ingeteam expanded these concepts with H6D1 and H6D2 configurations that balance diode placement for optimized transformerless string inverter performance.

For utility-scale PV plants, central inverters employ multilevel topologies such as two level VSI, three level NPC, and T-type converters are widely deployed. Mitsubishi has introduced asymmetric CHB topologies with unequal DC-link voltages to improve waveform quality and reduce switching frequency while maintaining transformerless design.

Finally, AC-module inverters like those from Enphase Energy and Siemens leverage interleaved flyback or resonant converters for high-frequency operation and modular scalability. These systems provide distributed Maximum Power Point Tracking (MPPT) and improved reliability, especially in shaded or segmented rooftop environments [39].

Another widely employed MLI configuration is the Series-Connected H-Bridge inverter, which features modular construction and scalable voltage capabilities. This topology is frequently adopted by Toshiba, Mitsubishi Electric, and Rockwell Automation in high-power applications requiring high redundancy and phase isolation. By connecting multiple H-bridge cells supplied through phase-shifted transformers, these systems achieve near-sinusoidal output waveforms with minimal filtering. Although they demand multiple isolated DC sources and complex transformer arrangements, Series-Connected H-Bridge-based inverters provide excellent harmonic performance and are ideal for utility-scale renewable energy systems and regenerative motor drives.

The FC inverter topology, while less common in medium voltage drives, finds niche use in test benches and high-speed industrial applications. Danfoss and Schneider Electric have explored FC-based MLIs for scenarios where symmetrical thermal distribution and high-frequency operation are advantageous. However, the requirement for large capacitances, complex voltage balancing mechanisms, and increased precharge demands limit their general use in low-frequency medium-voltage drives.

In pursuit of further improving power density and system simplification, hybrid topologies combining features of the NPC and Series-Connected H-Bridge

inverters have emerged. Such architectures, promoted in research and early prototypes by Hitachi and Fuji Electric, aim to reduce the number of required components while preserving output waveform quality. These hybrid systems exploit redundancy in switching states to enhance fault tolerance and simplify modulation control, providing a cost-effective alternative for high-power motor drives and grid-interface applications.

A critical challenge in medium-voltage power conversion is minimizing switching losses without degrading output waveform quality. Traditional high frequency switching methods introduce significant thermal stress and EMI, necessitating costly thermal management and filtering. To address this, modulation strategies are employed, enabling low-frequency operation (as low as 100 Hz) while maintaining THD within IEEE 519 standards. Firms have adopted these strategies to ensure reliable drive operation with reduced semiconductor stress, allowing the use of high-voltage devices like IGCTs and IGBTs with ratings up to 6.5 kV.

Transformerless medium-voltage drive systems represent a breakthrough in industrial inverter design. Traditionally, large and heavy isolation transformers were required to step down or galvanically isolate the grid from the motor. Recent developments by ABB, Siemens, and GE have led to transformerless designs based on dual three level NPC inverter configurations. These topologies eliminate transformers by using series-connected inverters sharing a common DC link and delivering phase voltages directly to the motor. Benefits include reduced system footprint, lower cost, enhanced efficiency, and simplified installation-attributes particularly desirable in offshore platforms, desert environments, and mobile industrial units.

From a system-level perspective, inverter design must also address issues such as common-mode voltage, EMI, and the insulation stress imposed on connected machinery. MLIs inherently reduce common-mode voltage due to smaller voltage steps, and when combined with appropriately designed Inductor-Capacitor (LC) filters or active damping circuits, they ensure minimal impact on motor windings and bearings. Industrial solutions, such as ABB's active front-end converters and Siemens' integrated filtering modules, further mitigate these effects and extend the lifespan of connected loads.

In conclusion, inverters are no longer auxiliary components but rather central to the design and operation of modern power systems. Their role extends far beyond energy conversion-they enable power quality control, system protection, grid compliance, and dynamic adaptability. With continuous advancements in semiconductor technology, modulation algorithms, and thermal design, MLI systems are shaping the future of industrial automation, renewable energy integration, and high-efficiency electric drives. The commitment of leading firms to commercialize and refine these technologies ensures that MLIs will remain at the forefront of sustainable and resilient power electronics [40].

In the modern EV industry, inverters are not just energy converters-they have evolved into key components that ensure efficient power delivery, control dynamic motor behavior, and enhance overall system reliability. The transition from conventional two-level VSIs to MLI topologies is gaining momentum, particularly due to the increasing shift toward 800 V DC-link architectures.

Porsche set a major benchmark with its Taycan, utilizing an 800 V battery system capable of handling charging powers up to 270 kW. This allowed the battery to reach 80% capacity in under 23 minutes, benefiting from lower current levels and improved conductor sizing-feasible only with advanced inverter design and control [40]. Lucid Motors went further with its Lucid Air, deploying over 900 V battery systems for fast charging and weight reduction [41].

Tesla, while primarily using 400 V systems, employs parallel-connected IGBTs in its two-level VSI design to meet high current demands, notably in the Model S and Model 3. However, this results in larger thermal footprints and packaging complexity, revealing the need for more scalable inverter structures [41], [42].

Toyota's Prius platforms have embraced compact integration by embedding dual VSIs and gate drivers directly into the transaxle unit. The fourth-generation Prius features a stacked modular design that minimizes interconnects and harness weight while enhancing thermal performance.

Nissan's LEAF, though relying on a conventional two-level structure, achieves high power output by paralleling IGBTs internally, highlighting a tradeoff between current handling and component count. Similarly, General Motors has implemented dual VSI topologies in the Chevrolet Volt and Cadillac CT6, where integration with

the drivetrain and use of liquid-cooled modules enable increased power densities beyond 15 kW/L [42].

Audi's A3 e-Tron, BMW's i3, and Hyundai's IONIQ 5 also illustrate brand-specific approaches to inverter design. Audi employs a Bosch-manufactured inverter with integrated thermal shielding and shared heat sinks, while BMW utilizes a dense six-pack IGBT module with modular cooling and control electronics. Hyundai, aligning with the IONITY alliance, has adopted 800 V MLIs to enable 350 kW fast charging, mirroring Porsche's approach.

Volkswagen and GM's latest models have begun incorporating modular MLI strategies to meet thermal and EMI constraints while maintaining scalability. Even in lower-voltage systems, such as the 400 V platforms in the Nissan LEAF, MLIs are being studied for future upgrades due to their inherent dv/dt suppression, harmonic mitigation, and enhanced switching efficiency.

In conclusion, traction inverter design in EVs is moving rapidly toward modular, multilevel configurations that leverage wide bandgap semiconductors, improve power density, and meet next-generation thermal and electrical demands. The combined commitment of industry leaders-including Porsche, Tesla, Toyota, Nissan, GM, BMW, Hyundai, Lucid, and Audi-clearly signals the rise of MLI systems as the backbone of sustainable and scalable e-mobility solutions [41], [42].

The strategic adoption of MMCs by industrial leaders such as Siemens and ABB has further emphasized the pivotal role of inverters in modern power electronics. Siemens' HVDC PLUS technology was first deployed in the Trans Bay Cable project, transmitting 400 MW over 88 km using a modular multilevel topology that proved its operational reliability and efficiency in a real-world scenario [43]. This converter design minimizes the need for bulky filters by achieving near-sinusoidal output waveforms, while maintaining low switching frequencies and THD, thus optimizing system performance. ABB has also pioneered MMC-based HVDC and voltage source converter (VSC) applications, notably in offshore wind integration and urban power delivery systems. For instance, ABB's installations such as the Gotland and Cross Sound projects demonstrate how compact, self-commutated converters can deliver high-quality power while reducing infrastructure footprint. In Germany's Energiewende context, VSC-based HVDC systems play a critical

role in transporting offshore wind energy to industrial centers inland, offering black-start capabilities, fast dynamic response, and reactive power support [44].

These implementations underline that inverters-particularly modular and multilevel variants-are foundational to grid modernization. The scalability, modularity, and harmonic performance of MMCs have not only transformed large-scale HVDC and FACTS deployments but have also opened pathways for multiterminal and meshed HVDC grids, a direction actively pursued by Siemens, ABB, and others [43], [44].

Beyond the foundational contributions of Siemens and ABB, various global firms have played integral roles in the proliferation and industrialization of MLI and HVDC technologies. ABB, for instance, pioneered the adoption of VSC technology in commercial HVDC applications with its Gotland project in 1999 and continued its leadership through systems like Cross Sound (330 MW) and the offshore Troll and Valhall platforms in Norway, enabling compact and high-efficiency solutions for remote oil and gas applications. In Japan, a joint venture by Hitachi, Toshiba, and Mitsubishi Electric resulted in one of the earliest back-to-back multiterminal VSC-HVDC systems, implemented at the Shin-Shinano substation. This 300 MW gate turn-off thyristor (GTO)-based converter marked a significant milestone in the evolution of self-commutated high-power inverters. China has emerged as another key innovator through firms such as Rongxin Power Electronic, NR-Electric, XiDian, and C-EPRI, leading large-scale deployments like the Nan'ao Island and Zhoushan VSC-HVDC systems. These networks feature three to five terminals and leverage MMC architectures to provide scalable and redundant energy transmission in areas with high renewable penetration [44].

In Europe, TenneT has spearheaded the integration of offshore wind farms using VSC-HVDC technologies, contributing to Germany's "Energiewende" targets. Collaborations with Siemens and ABB have resulted in robust infrastructure for transmitting wind power from the North Sea to inland load centers. Meanwhile, Transpower in New Zealand has deployed SVC PLUS systems from Siemens to improve voltage stability in remote grid nodes and continues to expand these efforts due to demonstrated success [43].

Together, these industrial efforts illustrate a global shift towards inverter-based grid control, highlighting how MLI and MMC topologies form the technological

backbone of not only energy conversion but also dynamic grid services, smart grid integration, and high-density power applications [43], [44].

In summary, inverters have evolved from basic energy conversion units into multifunctional, intelligent interfaces that are indispensable in modern power systems. Their roles span a wide range of applications-from distributed renewable energy integration and industrial motor drives to EVs and high-voltage transmission systems-underscoring their central importance in achieving reliable, efficient, and flexible grid operation. The technological advancements pioneered by leading firms such as ABB, Siemens, SMA, Mitsubishi, Hitachi, and others have not only shaped inverter topologies and control strategies but also enabled widespread deployment of MLI systems tailored to diverse operating conditions. As the energy landscape continues to shift towards higher penetration of renewables and electrified transportation, the inverter stands out as a cornerstone of smart, sustainable, and resilient power electronics. Continued research and industrial innovation will further enhance their performance, pushing the boundaries of efficiency, modularity, and system-level integration [39].

2.2 General Classification of Inverters

In power electronics, inverters are fundamental components used to convert DC into AC, serving as critical interfaces between energy sources and loads. Depending on their input characteristics and structural configurations, inverters are generally categorized into three main types: Current Source Inverters, Voltage Source Inverters, and Z-Source Inverters.

This section provides a comprehensive examination of these three inverter topologies, highlighting their structural properties, operational principles, advantages, and limitations. While CSI and VSI are considered traditional and widely implemented inverter types, ZSI represents an emerging solution that addresses certain limitations of the conventional configurations. The comparative analysis presented here aims to guide the selection of appropriate inverter architectures for specific application domains. Each topology will be further explored in detail in the following subsections.

2.2.1 Current Source Inverters

CSIs represent a class of power electronic converters that use an inductor as the primary energy storage component at the DC input side, rather than the capacitor-based architecture found in VSIs. This topology enables the inverter to operate as a constant current source, offering smooth current delivery and inherent short-circuit protection, which are particularly advantageous in grid-connected renewable energy systems such as PV applications [45].

CSIs typically exhibit higher reliability due to the long operational life of inductors and their ability to manage low and variable input voltages without requiring a separate DC-DC boost stage. This is especially beneficial for PV systems where input voltages can fluctuate significantly depending on environmental conditions. Furthermore, CSIs feature lower EMI and reduced dv/dt stress, improving their compatibility with sensitive loads and grid standards [46].

CSI architecture can be implemented in various configurations, including single-stage and multi-stage structures. Single-stage CSIs are favored for their simplicity, reduced component count, and high efficiency in low-to-medium power applications. In contrast, multi-stage CSIs provide enhanced output waveform control, scalability, and improved power quality, albeit with increased circuit complexity [45].

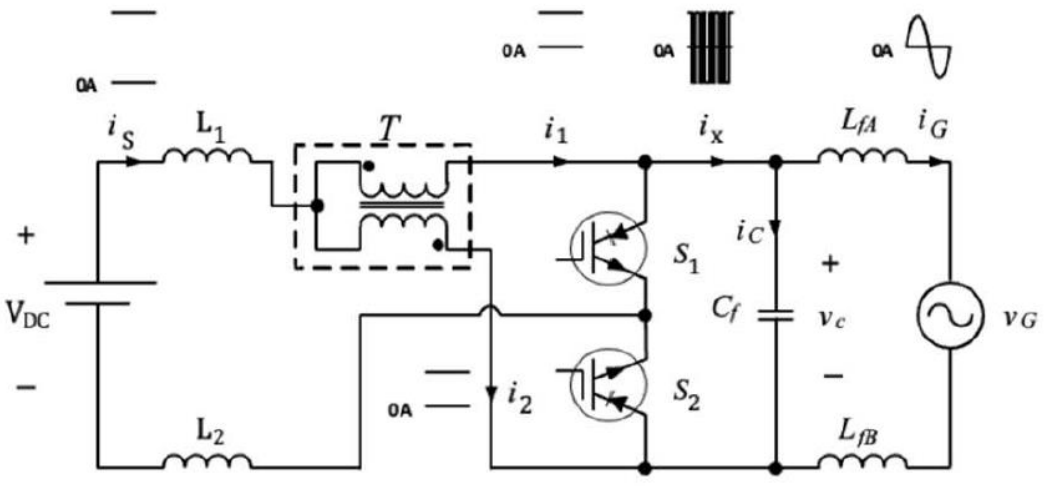


Figure 2.5 Half bridge CSI [46]

In recent developments, transformerless CSI topologies and half-bridge configurations -in the figure 2.5- utilizing reverse-blocking IGBTs have been

proposed to minimize component count and increase reliability while maintaining high efficiency. These advances aim to address traditional CSI limitations, such as bulky input inductors and harmonic distortion, making CSIs a competitive solution for next-generation smart grid and PV integration [46].

2.2.2 Voltage Source Inverters

Voltage Source Inverters are among the most widely used topologies in power electronic converters, particularly for grid-connected applications. Their operational principle is based on maintaining a stiff DC voltage at the input, typically regulated via a DC-link capacitor, and generating AC output voltages of variable magnitude and frequency using PWM techniques [47].

VSIs are advantageous due to their simple control structure, compatibility with space vector modulation (SVM), and capability to deliver high-performance voltage waveforms. However, they inherently lack short-circuit protection and bidirectional power flow unless paired with additional components such as a bidirectional rectifier [47].

In low and medium voltage systems, VSIs often include Inductor-Capacitor-Inductor (LCL) filters to minimize output harmonic distortion. Moreover, in systems utilizing renewable energy sources like PV or wind energy, a DC-DC converter is generally required to boost the variable input voltage to the fixed level required by the VSI, which increases the complexity and cost of the system [47].

In terms of semiconductor stress, each switching device in a VSI experiences the full DC-link voltage in the off-state and the peak line current in the on-state. Devices such as IGBTs with anti-parallel diodes are typically used to meet these requirements. The effectiveness of modulation techniques like SVM allows for better DC voltage utilization, enabling the inverter to operate with approximately 15% lower DC voltage compared to SPWM [47].

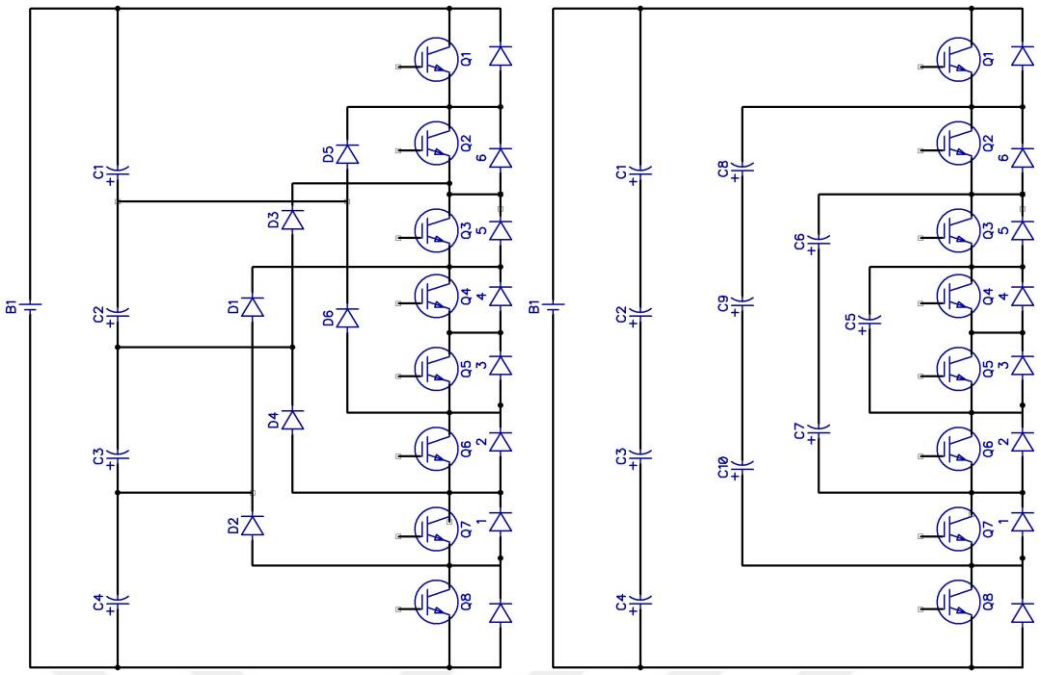


Figure 2.6 (a) NPC MLI (b) FC MLI [48]

Figure 2.6 illustrates two prominent voltage source-based MLI topologies. Part (a) presents the NPC MLI, where multiple DC-link capacitors and clamping diodes are employed to achieve stepped voltage levels. In contrast, part (b) depicts the FC-Based MLI, which utilizes capacitors in a floating configuration to generate intermediate voltage levels [35].

In high-power drive applications, VSIs present clear structural and functional advantages over CSIs. VSI systems require only a simple diode-bridge front end, offering minimal cost and high reliability, whereas CSIs need a controlled current source with an active front-end converter, increasing system complexity and cost [36].

Furthermore, VSIs maintain high efficiency even at light loads due to flexible modulation strategies. Conversely, CSIs must operate with a fixed nominal current to preserve torque capacity, which leads to excessive conduction and switching losses at low load conditions. Studies have shown that while a VSI can achieve efficiencies of around 93% at 10% load, a CSI might drop as low as 60% under similar circumstances [49].

Additionally, CSI systems rely on large and heavy DC-link inductors that result in significant size, weight, and thermal losses. VSIs, in contrast, use capacitive energy

storage, which is more compact and has minimal power loss. These design efficiencies make VSIs an attractive solution for modern power conversion systems, especially in renewable integration and high-efficiency industrial drives [49].

Despite their benefits, VSIs exhibit limitations such as higher dv/dt, higher THD, and an inability to provide implicit voltage boost. However, their modularity and adaptability to multilevel converter structures like NPC and CHB make them well-suited for medium-voltage industrial drives and high-power applications [50].

Recent advances have further enhanced VSI performance through systematic design optimization methodologies. Specifically, the development of optimization tools based on analytical modeling and evolutionary algorithms has enabled the minimization of system size and cost while satisfying key operational constraints such as thermal limits, switching losses, and EMI standards. For instance, in industrial motor drive applications, optimal selection of components such as IGBTs, DC-link capacitors, and EMI filters has been shown to significantly improve inverter efficiency and reliability. Additionally, integrated optimization approaches allow for the coordinated design of thermal management systems and filter structures, ensuring compliance with EMI regulations and thermal derating requirements [51].

2.2.3 Z-Source Inverters

Z-Source Inverters are an innovative power conversion topology developed to overcome the inherent limitations of conventional VSIs and CSIs. Utilizing a unique impedance network composed of two inductors and two capacitors, ZSIs can achieve both voltage boost and buck operations in a single-stage structure. One of their key distinctions is the controlled use of the shoot-through state-normally prohibited in traditional inverters-which significantly enhances reliability and extends voltage gain range [52], [53], [54].

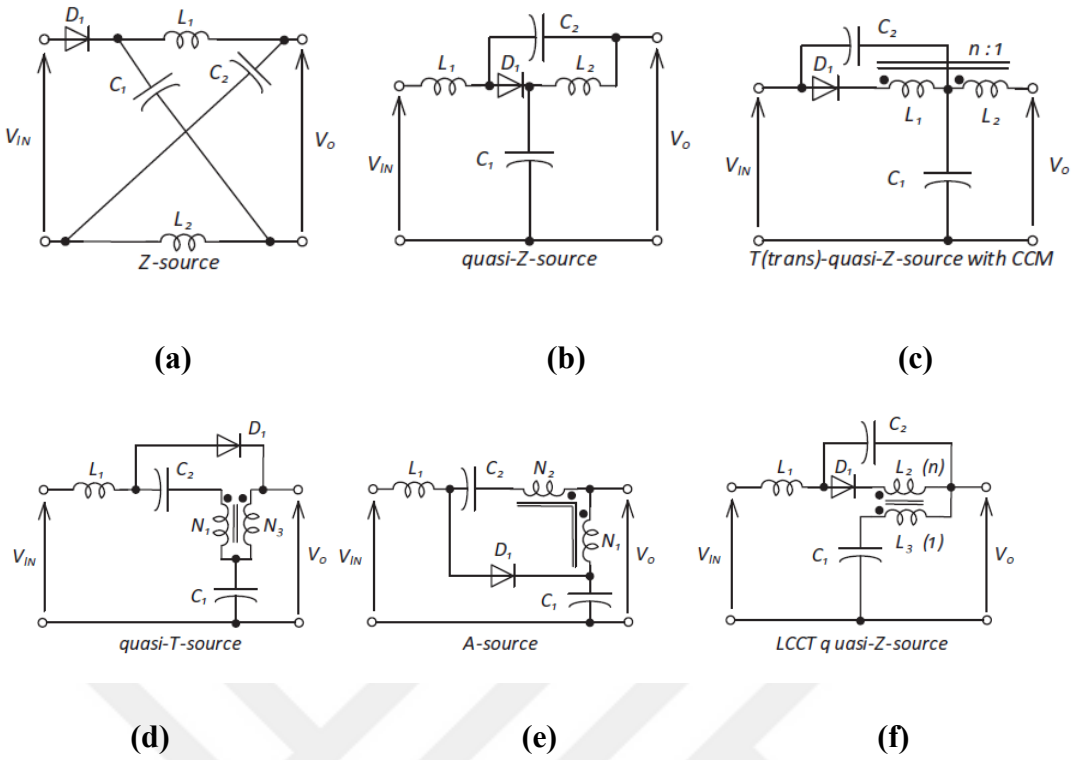


Figure 2.7 Generalization of the impedance-source networks: (a) Z-source; (b) quasi-Z-source; (c) Trans-quasi-Z-source; (d) quasi-Trans-source; (e) A-source; and (f) Inductor–Capacitor–Coupled Transformer quasi-Z-source [55]

Figure 2.7 illustrates a range of basic and magnetically coupled Z-source networks. The original Z-source network is shown in Fig. 2.4a, followed by the quasi-Z-source network in Fig. 2.4b, which provides continuous input current and utilizes passive components of similar size and volume to the conventional ZSI. The topologies in Figs. 2.4c to 2.4f represent magnetically coupled impedance-source networks. The T-quasi-Z-source network (Fig. 2.4c) is the first of these, featuring coupled inductors with continuous input current. Although it includes an additional capacitor, previous studies have shown that the total capacitor volume remains lower. The quasi-T-source network (Fig. 2.4d) also provides continuous input current and has a slightly different structure. The A-source network (Fig. 2.4e) is one of the most recently proposed configurations, while the LCCT network (Fig. 2.4f) exhibits similar operational characteristics.

All magnetically coupled impedance-source topologies offer enhanced voltage boost capability due to the transformer turns ratio, which enables a shorter shoot-through duty cycle. However, the specific impact of this reduction on converter size and cost has not yet been clearly addressed in the literature [55].

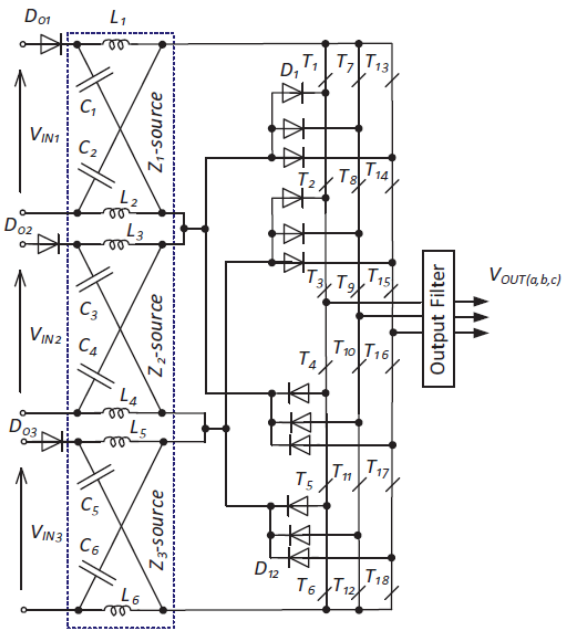


Figure 2.8 4-level ZSI of NPC [55]

Figure 2.8 illustrates a four-level buck/boost inverter, wherein each input power source is apportioned across several impedance-source networks. This concept exemplifies how any impedance-source network can be extended to a MLI using a diode clamped approach. Since each Z-source allows for independent regulation of its output voltage, such MLIs are particularly well-suited for power supply systems with locally dispersed energy sources [55].

Among the notable advantages of ZSIs are their ability to operate without an auxiliary DC-DC converter, reduced component count, improved EMI immunity, and high efficiency due to single-stage energy conversion. These features make them particularly appealing for renewable energy systems such as PV arrays, fuel cells, and electric traction systems, where wide input voltage variation is common [52], [54].

However, ZSIs also come with certain drawbacks. The presence of shoot-through states can increase switching losses and introduce additional harmonic distortion. Furthermore, the voltage and current stresses on passive components complicate the design and selection process. When high boost ratios are achieved using coupled inductors, EMI and magnetic coupling issues may arise, requiring careful hardware design and filtering considerations [52], [53].

Therefore, while ZSIs present an attractive solution for specific applications, their complexity, component stress, and control challenges make them less ideal for systems demanding simplicity, high reliability, and low cost.

In this context, VSIs continue to be the most widely adopted topology in power electronics due to their straightforward design, efficient control strategies, and robust performance under steady DC input conditions. The next section will present a detailed classification of VSI topologies, exploring their advantages, use cases, and comparisons for various application environments.

2.3 Classification of Voltage Source Inverters

Voltage Source Inverters are fundamentally categorized into two principal structural types: two-level inverters and multilevel inverters. This classification serves as the foundation for analyzing their respective operational principles, modulation strategies, advantages and limitations, and various application areas, which will be discussed in the following sections.

2.3.1 Two-Level Inverters

A two-level voltage-source inverter represents the most fundamental configuration within inverter technology. It generates an output voltage that alternates between two discrete levels, typically corresponding to the positive and negative poles of a DC source. This binary switching operation forms a square waveform across the load. Although simple in structure and control, two-level inverters are limited in high-power applications due to the large voltage stress on switching devices and higher harmonic content in the output waveform.

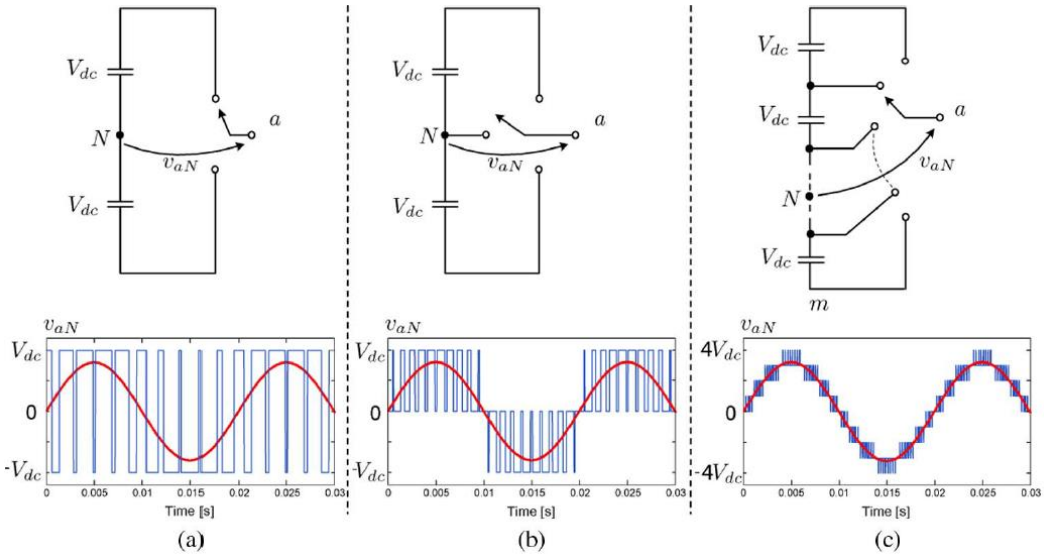


Figure 2.9 One phase leg of a VSI with two, three, and n output levels [2]

Figure 2.9 illustrates the schematic representation of a single-phase leg of voltage-source inverters for different output level configurations:

- In part (a), the two-level inverter alternates the output between two voltage states.
- In part (b), the three-level inverter introduces an intermediate voltage level, enabling a stepped waveform.
- In part (c), a generalized n-level inverter is depicted, where multiple discrete voltage levels are synthesized, forming a staircase-like output. This progression clearly demonstrates how increasing the number of levels enhances the output waveform resolution, reducing THD and improving power quality.

MLIs have emerged as a compelling solution to overcome the limitations of conventional two-level and three-level inverter topologies in medium- and high-power applications. A fundamental advantage of MLIs lies in their ability to synthesize output voltages that more closely approximate an ideal sinusoidal waveform using multiple discrete voltage steps. This concept is illustrated in the figure above, where different inverter structures-(a) two-level, (b) three-level (e.g., NPC), and (c) higher-level cascaded or hybrid multilevel-generate output waveforms with increasing voltage resolution.

In the two-level inverter configuration (Fig. 2.6 a), the output voltage alternates between only two discrete levels: $+V_{dc}$ and $-V_{dc}$. This results in a quasi-square

waveform with high THD, as seen in the stair-stepped pulse pattern far from the reference sine wave. Such waveforms demand extensive filtering to meet power quality standards.

As depicted in Fig. 2.6 (b), introducing a third voltage level (e.g., 0 V via a neutral point in a three-level NPC inverter) allows for an intermediate step in voltage synthesis. This reduces the amplitude of voltage steps and improves the approximation of the reference sinusoidal waveform. Consequently, harmonic distortion is significantly reduced, and the output waveform exhibits lower dv/dt stress, benefiting connected loads.

In Fig. 2.6 (c), an MLI with even higher levels (e.g., five-level or more via CHB or hybrid topologies) is shown. Here, the number of discrete voltage steps increases further, and the synthesized output waveform becomes markedly closer to a true sinusoid. As the number of levels increases, the step height between adjacent voltage levels decreases, enabling smoother transitions and finer resolution. This results in reduced THD, minimized filtering requirements, and improved electromagnetic compatibility.

Mathematically, the harmonic content of the output voltage decreases approximately inversely with the number of levels. Specifically, for an ideal N_{level}-level inverter, the number of steps per half cycle is N_{level} -1, and the THD can be approximated to decrease proportionally with 1/ N_{level} under certain modulation schemes. Therefore, increasing the level count is a direct and effective strategy to enhance waveform quality while enabling low switching frequency operation, which in turn reduces switching losses and improves overall inverter efficiency [56], [57].

Recent advancements in multilevel inverter topologies aim to maximize the number of output levels by utilizing various combinations of multiple DC sources with optimized switching strategies. The configurations enable the synthesis of finely stepped voltage waveforms using fewer power switches, which not only improves harmonic performance but also reduces device count and conduction losses. These improvements, combined with tailored modulation schemes, offer enhanced waveform quality at low switching frequencies, making the approach suitable for high-voltage and high-power applications [58].

In conclusion, the progressive improvement in output waveform fidelity with increasing inverter levels, as demonstrated in the figure, underscores the critical role of multilevel topologies in meeting the stringent waveform quality, efficiency, and reliability demands of modern power electronic systems.

2.3.2 Multilevel Inverters

MLIs, more precisely known as multilevel voltage-source inverters, are power electronic converters designed to synthesize stepped voltage waveforms by combining multiple voltage levels at their output. Unlike conventional two-level inverters that generate only high and low voltage states, MLIs can produce multiple discrete voltage levels, resulting in a staircase-like waveform that closely approximates a sinusoidal output [1], [59].

The emergence of MLIs was driven by the increasing demand for high-power and medium-voltage applications where traditional topologies were limited by switching losses, device voltage ratings, and harmonic performance. MLIs overcome these limitations by distributing voltage stress among multiple power semiconductors and reducing THD without requiring high-voltage-rated components.

Three primary MLI topologies dominate the literature and industry:

- NPC or Diode-Clamped inverters, which use clamping diodes to limit device voltage stress and are suitable for industrial drives.
- FC inverters, which offer natural voltage balancing through strategically placed capacitors.
- CHB inverters, which connect multiple single-phase H-bridge cells in series, typically powered by isolated DC sources, allowing for modular and scalable implementations [59], [60].

Each topology offers distinct trade-offs. For instance, NPC inverters are robust but require complex neutral-point voltage control. FC topologies simplify balancing but involve high capacitor counts. CHB inverters are highly modular and fault-tolerant but depend on multiple isolated sources. Despite these challenges, MLIs are widely used due to their superior output waveform quality, reduced EMI, and lower switching frequency requirements [1], [59], [60].

The continued evolution of MLIs has been accompanied by the development of advanced modulation strategies such as multicarrier PWM, SVM, and SHE. These techniques exploit the increased number of switching states in MLIs to optimize performance and minimize THD [59], [60]. As highlighted by Franquelo et al., MLIs have transitioned from a promising research area to mature technologies deployed in a broad range of applications, including renewable energy systems, EVs, high-performance motor drives, and smart grid integration [60].

2.4 Transition from Two-Level to Multilevel Inverters

As power electronic applications continue to expand in scale and complexity, the limitations of traditional two-level inverter systems have become increasingly evident. Initially dominant in industrial motor drives and low-voltage systems, two-level inverters now struggle to meet the stringent demands of modern power conversion-particularly in medium-voltage and high-power environments [59]. Their binary nature results in excessive voltage stress, high harmonic distortion, and limited waveform shaping capabilities, all of which challenge their effectiveness in contemporary applications [1].

To address these constraints, the field has witnessed a significant transition toward MLI topologies. MLIs produce output voltages with multiple discrete levels, thereby improving waveform quality, reducing switching losses, and facilitating efficient high-power operation without the need for high-voltage-rated devices [59], [60]. This shift represents more than just a topological evolution-it reflects a growing necessity for high-resolution voltage synthesis, improved electromagnetic compatibility, and modular converter structures suited to the needs of modern energy systems.

The following subsections elaborate on the key limitations of two-level inverters and explore the fundamental motivations behind the adoption of multilevel structures, with a particular emphasis on the demand for enhanced voltage resolution, power quality, and system scalability.

2.4.1 Limitations of Two-Level Inverters

Two-level VSIs have historically dominated the landscape of low-power and general-purpose applications due to their simple topology and ease of control. However, their inherent limitations become pronounced when extended to medium-

voltage and high-power environments. The fundamental constraint lies in their binary switching behavior, where the output voltage can only toggle between two discrete levels, typically $+V_{dc}$ and $-V_{dc}$. This results in a quasi-square waveform that contains significant harmonic content, particularly low-order harmonics, which adversely affect power quality and motor performance [59].

To attenuate these harmonics and meet IEEE 519 harmonic standards, large passive filters-especially bulky LC filters-are required at the output. These filters not only increase the overall size and cost of the inverter system but also introduce resonance issues and dynamic limitations in fast-changing load conditions [1]. Furthermore, when connected to induction motors, the high dv/dt associated with two-level switching induces additional stress on motor insulation and can cause bearing currents, potentially leading to premature equipment failure [1].

Another critical drawback is the voltage stress borne by the semiconductor switches. In a two-level inverter operating in medium-voltage ranges, each switch must withstand the full DC bus voltage, often exceeding 2.3 kV in industrial drives. This directly translates to higher switching losses and thermal stress, which in turn necessitate sophisticated cooling and protection mechanisms. Such high dv/dt transitions also exacerbate EMI, posing challenges for compliance with electromagnetic compatibility directives [1], [59].

To mitigate the output voltage distortion, increasing the switching frequency is a common strategy. However, this approach leads to an exponential rise in switching losses, particularly in medium-voltage -rated power devices such as IGBTs and IGCTs, whose losses are not negligible at elevated frequencies. Consequently, the efficiency of the inverter system deteriorates, and the permissible power density is significantly reduced [59].

Scalability is another area where two-level inverters fall short. While parallel or series configurations of power devices can theoretically extend voltage or current handling capabilities, they introduce complex control requirements and non-uniform current or voltage sharing, which may cause reliability issues or device derating. Additional balancing circuits and snubber networks are required to maintain operational integrity, further increasing system complexity and cost [1].

Given these limitations, two-level inverters are often deemed unsuitable for advanced medium-voltage industrial applications, where performance requirements are stringent and system robustness is critical. These challenges have led to the development and widespread adoption of MLI topologies, such as the NPC, FC, and CHB, which offer improved waveform quality, reduced switching losses, and enhanced modularity for high-power systems [59].

2.4.2 Motivations for Transition to Multilevel Inverters in Modern Power Electronics

In modern power electronics, particularly in medium-voltage and high-power applications, achieving precise and high-quality output waveforms is a fundamental requirement. This demand stems from increasing constraints on THD, electromagnetic compatibility, and efficiency imposed by both international standards and application-specific needs. Two-level inverter topologies, while historically dominant, exhibit considerable limitations in synthesizing sinusoidal voltage waveforms due to their binary switching nature. As a result, high-resolution voltage synthesis has emerged as a key enabling technology to fulfill these stringent power quality expectations [61].

To meet stringent power quality and efficiency requirements in modern electrical systems, high-resolution voltage synthesis has become essential. MLIs address this demand by producing output voltages that closely approximate a sinusoidal waveform through a series of discrete voltage steps [59]. This significantly reduces the THD and associated EMI, even without complex filtering techniques. Additionally, MLIs enable operation at lower switching frequencies while maintaining high output fidelity, thus minimizing switching losses [1]. The ability to tailor the number of levels allows for enhanced control flexibility and design optimization in diverse applications ranging from traction systems to renewable energy integration [3]. Hence, the shift toward multilevel structures is not merely evolutionary but a necessity dictated by the operational constraints and performance expectations of today's power systems [59], [60].

MLIs have been developed specifically to meet this requirement by producing output waveforms through multiple discrete voltage levels. This stepwise approximation significantly improves the fidelity of the output voltage, closely

resembling a pure sinusoidal signal and drastically reducing low-order harmonic content. Compared to traditional two-level inverters, the reduced harmonic spectrum lowers the thermal and electromagnetic stress on both power components and connected loads, including induction motors and transformers. This inherently reduces the need for large and complex filtering solutions at the output stage.

Moreover, the use of MLIs facilitates inverter operation at lower switching frequencies, often below 100 Hz, without compromising the output waveform quality. This is a critical advantage in medium-voltage systems where switching losses account for a significant portion of total power losses. By synthesizing a near-sinusoidal waveform with minimal switching transitions, MLIs effectively lower the cumulative switching and conduction losses in power semiconductor devices such as IGBTs and IGCTs.

An additional benefit of multilevel structures lies in their scalability and configurability. The number of voltage levels can be tailored according to specific system requirements, offering enhanced design flexibility and modulation strategies. This adaptability is particularly advantageous in applications such as grid-connected renewable energy sources, high-speed drives, electric traction systems, and active power filters, where operational dynamics vary widely.

The precise control over voltage waveforms offered by MLIs also contributes to mitigating common-mode voltages and dv/dt-induced stress on motor windings, ultimately extending the service life of electrical machinery. In systems requiring transformerless operation, such as offshore platforms or compact industrial installations, the fine granularity in voltage synthesis allows for high-quality power delivery without additional isolation or filtering stages [61].

In summary, the transition to high-resolution voltage synthesis using MLIs is not simply an advancement in converter design but a necessary response to the evolving demands of high-performance, high-efficiency electrical systems. The ability of MLIs to deliver superior waveform quality, lower losses, and operational flexibility underscores their central role in the future of power electronics.

In modern power electronic systems, particularly in medium-voltage and high-power transportation applications, the transition from two-level to MLI has become critical to achieve high-resolution voltage synthesis. Conventional two-level

inverters struggle with increasing DC-link voltages due to their limited ability to synthesize near-sinusoidal waveforms, resulting in higher THD, switching losses, and EMI [48]. To overcome these limitations, MLIs enable the generation of stepped voltage waveforms using lower-rated semiconductor devices, thus allowing better voltage resolution, reduced switching frequency, and improved efficiency.

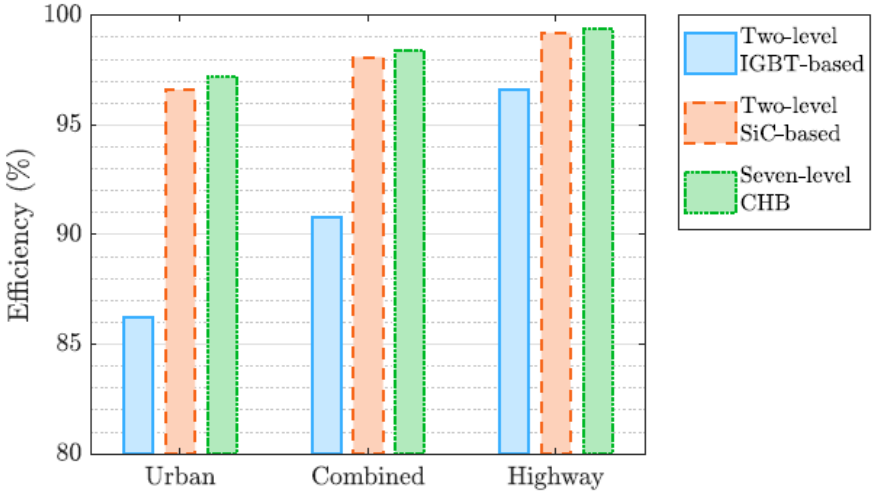


Figure 2.10 Comparative efficiency analysis of two-level and multilevel converter topologies [64]

These advantages are not only theoretical but have been practically realized in industrial applications. The widespread adoption of two-level inverters in early EV architectures, as evidenced in vehicles from major manufacturers such as Audi, Toyota, Nissan, Chevrolet, and Tesla, underscores their reliability and design simplicity in low-voltage systems (typically 400 V) [62],[63]. These conventional topologies have proven effective in earlier EV generations, particularly when leveraging silicon IGBT technology. However, as the industry shifts toward higher DC-link voltages - primarily 800 V and above- to support ultra-fast charging, reduced cabling weight, and enhanced power density, the limitations of two-level structures have become increasingly apparent [62], [64].

To address the growing need for efficient, high-voltage operation and reduced EMI, wide-bandgap devices such as Silicon Carbide (SiC) Metal Oxide Semi-conductor Field Effect Transistors (MOSFETs) have been introduced into two-level inverter designs. Although wide-bandgap devices offer superior switching performance and lower conduction losses, they alone are insufficient to mitigate the intrinsic

shortcomings of two-level topologies-particularly in handling high dv/dt, increased switching losses, and limited output voltage resolution [62], [63], [64].

MLI topologies such as NPC, CHB, and MMC have thus gained significant traction, especially in high-power traction applications including electric trains, marine propulsion, and emerging high-performance EV platforms [64]. These topologies inherently enable finer voltage steps, resulting in better output waveform quality, reduced THD, and minimized voltage stress on switching devices. Furthermore, they provide enhanced scalability and modularity, making them highly suitable for future-proof vehicle designs operating at elevated voltage levels.

Costs	Two-level Inverter	7-Level CHB Inverter
Switches	296.6	203.4
Gate Drivers	39	234
Capacitors	30.3	0
Heatsink	17.3	16.2
Controller	150	300
Battery	5760	5310
Contactor	74	180
Overhead Cost	133.3	188.6
Sum	6500.5	6433.3

Figure 2.11 Cost analysis between multilevel and two-level inverter architectures [63]

Empirical studies and industrial implementations demonstrate the practical efficiency gains achieved by MLIs. For instance, Figure 2.10 in [64] demonstrates that the seven-level CHB MLI consistently achieves higher efficiency than both IGBT- and SiC-based two-level inverters across urban, combined, and highway driving conditions - most notably in urban scenarios where higher switching frequencies amplify the benefits of finer voltage resolution.

In addition, cost comparisons shown in Figure 2.11 of [63] reveal that despite their higher component count and complexity, MLIs may lead to overall cost optimization when considering the reduced need for paralleling devices, cooling requirements, and EMI mitigation.

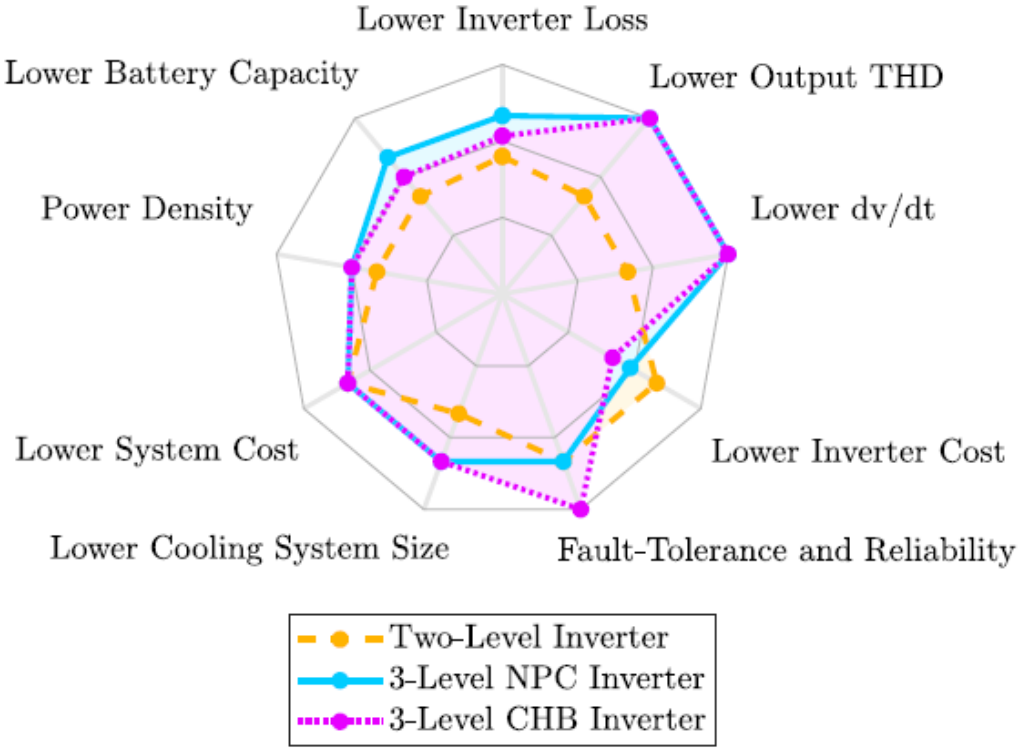


Figure 2.12 Comparative performance analysis of two-level and three-level inverter topologies based on key operational metrics [64]

Beyond efficiency and cost considerations, MLI topologies also offer advantages across a broader set of performance metrics. As illustrated in Figure 2.12 of [64], when conventional two-level inverters are compared with three-level NPC and three-level CHB configurations, multilevel designs demonstrate superior performance in terms of power quality, fault tolerance, and electromagnetic compatibility. While two-level inverters retain simplicity and lower control complexity, multilevel alternatives notably reduce output voltage distortion and switching stress, thereby enhancing reliability and operational safety. This comprehensive comparative analysis further reinforces the suitability of MLIs for high-performance EV applications, where multi-criteria optimization is essential.

In summary, as EV powertrains evolve to meet higher voltage and performance demands, high-resolution voltage synthesis offered by MLIs presents a compelling alternative to traditional two-level architectures. Their adoption is no longer just a theoretical consideration, but a tangible trend reflected in industrial progress and system-level performance metrics [63], [64].

Moreover, the ability to operate MLIs at lower switching frequencies while still achieving high waveform fidelity reduces thermal stress on semiconductors and lowers filter requirements. Additionally, the modular and scalable nature of multilevel converters supports future EV architecture and facilitates design optimization across varying power levels and application-specific constraints.

Thus, high-resolution voltage synthesis through MLIs represents not merely a technological improvement, but an industry-driven response to the rising demands for high-efficiency, low-EMI, and high-voltage power conversion in electric mobility and transportation electrification [62], [63], [64].

Consequently, multilevel topologies such as NPC, CHB, and MMC have found widespread adoption in high-power transportation systems including railway drives and electric ship propulsion, where higher voltage levels are essential.

A prominent example is the TRANSRAPID Maglev system, where three-level GTO-based inverters with modular control architectures were developed and tested under real-world conditions. These converters demonstrated the ability to generate high-fidelity sinusoidal output waveforms at fundamental frequencies approaching 300 Hz, without compromising on AC voltage or current, even during asynchronous modulation. This system architecture, including double-end power feeding and drive control zones, validates the feasibility and necessity of multilevel voltage synthesis for next-generation transport solutions [65].

Traditional two-level inverter structures have proven inadequate for medium-voltage and high-power marine propulsion systems, primarily due to inherent drawbacks such as high switching losses, EMI, limited output voltage quality, and poor reliability. In such systems, maintaining acceptable waveform quality necessitates high switching frequencies, which in turn lead to increased thermal stress on semiconductor devices, higher cooling demands, and greater system complexity and volume. Furthermore, a single point of failure in these systems results in complete shutdown, posing significant challenges for applications requiring uninterrupted operation. In response to these limitations, more advanced converter structures have emerged, offering not only improved energy conversion efficiency but also advantageous features such as lower harmonic distortion, reduced common-mode voltage, minimized voltage stress on devices, modularity,

reconfigurability, and fault tolerance at the system level. These architectures are particularly well-suited to meet marine-specific regulatory requirements, including those defined by IEEE Std. 45-2002, which emphasizes low harmonic distortion and reliable continuous operation in electric shipboard systems [66].

Traditional two-level inverter-based Static Synchronous Compensator (STATCOM) systems are inherently limited in addressing complex transmission-level issues such as active power imbalances, transient stability, and sub synchronous oscillations, as they primarily offer reactive power control. To overcome these limitations, STATCOM architectures integrated with energy storage systems have been proposed. However, the use of high-voltage battery stacks in conventional configurations often leads to instability due to series connection constraints. In this context, integrating multilevel converter topologies enhances system stability by enabling the use of lower-voltage storage units while improving voltage quality. Specifically, NPC and cascaded MLIs offer key advantages such as reduced switching losses, minimized harmonic distortion, and enhanced modulation capabilities. Their application in STATCOM/energy storage systems enables not only reactive but also dynamic active power control, thus providing a more comprehensive and effective solution for modern transmission networks [67].

Although conventional two-level inverters are widely used in low-power applications due to their cost-effective nature, they fall short in medium-voltage and high-power adjustable speed drive systems in terms of power density and energy efficiency. The increasing demand for advanced motor control, regenerative capability, and grid interaction has accelerated the adoption of MLI architectures in high-power applications. These multilevel structures can deliver high-quality output at reduced switching frequencies, significantly lowering THD and minimizing the need for bulky filters. Moreover, as voltage levels increase, the stress on individual semiconductor devices is reduced, enabling safer and more scalable converter designs. Advances in power semiconductor technology and the rise of modular design concepts have further facilitated this transition. In practice, meeting power quality standards such as IEEE 519 not only involves harmonic mitigation but also requires compatibility with utility networks, making multilevel solutions increasingly essential. Therefore, the transition from two-level to MLIs

represents not merely a technological upgrade, but a vital step toward sustainability and operational efficiency in industrial power systems [68].

Although traditional two-level VSCs were initially central to HVDC system implementation, their inherent limitations-such as elevated switching losses, high harmonic content, and extensive filtering requirements-have driven the transition toward more advanced MLI topologies. Two-level inverters struggle to meet the demands of high-voltage, high-power transmission, especially in terms of waveform quality and efficiency. In contrast, multilevel converter structures-such as NPC, FC, and MMC-offer improved voltage resolution and lower harmonic distortion. The NPC topology, while reducing voltage stress on switching devices through its three-level structure, faces challenges in voltage balancing among dc-link capacitors and uneven power loss distribution. FC topologies support greater voltage levels but require complex control and a high number of capacitors. The MMC, with its cascaded submodule configuration, provides scalable design and reduced switching frequency losses, eliminating the need for large filters. These attributes have solidified the role of multilevel topologies in modern HVDC transmission, where two-level approaches are no longer sufficient for meeting stringent performance and integration requirements [69].

Multilevel converter topologies have emerged as a key solution in response to increasing power demands and efficiency targets in wind turbine systems. Compared to conventional two-level converters, multilevel configurations offer reduced harmonic content in both input and output voltages, lower EMI, and the capability to operate at significantly reduced switching frequencies. This leads to less demanding input filtering and considerable reduction in switching losses. For instance, a multilevel converter can achieve similar harmonic performance to a two-level converter while operating at just 25% of the switching frequency, thus improving efficiency. However, one commonly reported drawback in split DC-link multilevel converters is the voltage imbalance among capacitors. This issue can be mitigated either by incorporating additional hardware or by modifying the reference voltage through a model-based software control approach. Furthermore, by utilizing multipole low-speed generators with multiple windings, independent DC sources can be derived to realize cascaded structures. Each stage can then be configured as a power-electronic building block comprising a rectifier, a DC link, and an H-

bridge. Such modular configurations enable direct connection of the wind turbine converters to the wind-farm distribution network, eliminating the need for bulky transformers. The ongoing reduction in the cost per kilowatt of power-electronic building blocks further supports the widespread industrial adoption of cascaded multilevel topologies [70].

Two-level inverters have demonstrated significant limitations, especially in high-power applications, due to their low output voltage quality, high THD, and the necessity for bulky output filters. These drawbacks have catalyzed the adoption of MLI topologies, which offer improved efficiency, compatibility, and compactness in grid-connected PV systems. Topologies such as the three-level NPC, three-level T-type, and asymmetric CHB enable the generation of multiple discrete voltage levels at the inverter output, thus allowing low-distortion waveforms without increasing the switching frequency. This reduces the size and cost of passive filters while minimizing the total power losses across the conversion stages. Furthermore, multilevel designs can eliminate the need for input-side boost converters or output-side step-up transformers, streamlining the power path and enhancing overall system efficiency and thermal performance. Notably, in topologies like the CHB, PV arrays can be independently controlled via separate MPPT algorithms, offering superior performance under partial shading or mismatch conditions. These advantages have extended the application of MLIs beyond large-scale PV plants into residential and rooftop PV installations, reinforcing their relevance in the ongoing evolution of PV converter technology [71].

In conclusion, the inherent limitations of conventional two-level inverter structures render them insufficient for meeting the increasing demands of modern high-performance and high-voltage systems, thereby necessitating the adoption of MLI topologies. Expectations such as enhanced power density, reduced harmonic distortion, improved electromagnetic compatibility, and flexible modulation capabilities have positioned multilevel architectures not merely as an alternative, but as an indispensable solution in advanced power electronic systems. The following chapter will delve into the fundamental principles, architectural variants, and application domains of MLIs in greater technical depth.

3
MULTILEVEL INVERTER TECHNOLOGY: TOPOLOGIES, MODULATION STRATEGIES, AND INDUSTRIAL APPLICATIONS

This chapter provides an in-depth exploration of MLI technology, which has emerged as a critical advancement in the field of power electronics. MLIs are widely recognized for their ability to synthesize high-quality output voltages with reduced harmonic distortion, lower EMI, and improved voltage ratings, making them ideal for medium to high-power applications. The chapter commences with a general overview of MLIs and proceeds to detail their various topological classifications, including conventional configurations, ANPC MLIs, MMCs, hybrid structures, and RSC-MLI variants.

Following the topological discussion, attention is given to modulation strategies employed in MLIs, ranging from fundamental switching frequency techniques to high-frequency modulation schemes designed to optimize THD and system performance. The practical deployment of MLIs across a wide range of industrial and renewable energy applications is then examined, highlighting their significance in sectors such as PV systems, EVs, HVDC transmission, and smart grids. In addition, the chapter reviews relevant literature concerning power losses and efficiency characteristics of MLI systems. It concludes by summarizing key findings and identifying prevailing research gaps, thus laying a foundation for future investigations into next-generation inverter designs.

3.1 Overview of Multilevel Inverters

MLIs have become a fundamental component in the field of power electronics, particularly owing to their ability to produce output voltages with improved waveform quality, minimized harmonic distortion, and enhanced energy efficiency. Unlike conventional two-level inverters that switch between only two voltage levels, MLIs utilize multiple discrete voltage steps, resulting in a staircase-like waveform that approximates a sinusoidal signal more effectively. This feature not only reduces THD but also improves electromagnetic compatibility and reduces stress on power devices. Consequently, MLIs are extensively employed in medium-

and high-power domains - such as aerospace applications - owing to their superior voltage quality, reduced EMI, and enhanced energy efficiency [72].

The following sections of this chapter will delve deeper into these MLI topologies. In addition, modulation strategies, THD reduction techniques, application-specific considerations, and power loss-efficiency analysis will be comprehensively reviewed. The chapter will conclude with a synthesis of the key findings and highlight existing research gaps to guide future investigations.

3.2 Multilevel Inverter Topologies

Voltage Source Inverters are commonly divided into two primary categories: traditional two-level inverters and MLIs. MLIs have gained significant attention in medium- and high-power applications due to their ability to produce stepped output waveforms with lower harmonic content and reduced voltage stress on power devices. This structural evolution has led to a variety of topologies, each offering unique benefits and trade-offs.

As illustrated in Figure 3.1, MLIs are categorized based on their topology and the number of required DC sources. Topologies such as the NPC, FC, MMC, and ANPC inverters are designed to operate with a single DC source, which simplifies their power supply structure. In contrast, the CHB MLI, Hybrid MLI, and RSC-MLIs require multiple isolated DC sources, which enable modular design but introduce additional challenges in voltage balancing and control. These distinctions critically affect switching complexity, system efficiency, and overall reliability [73].

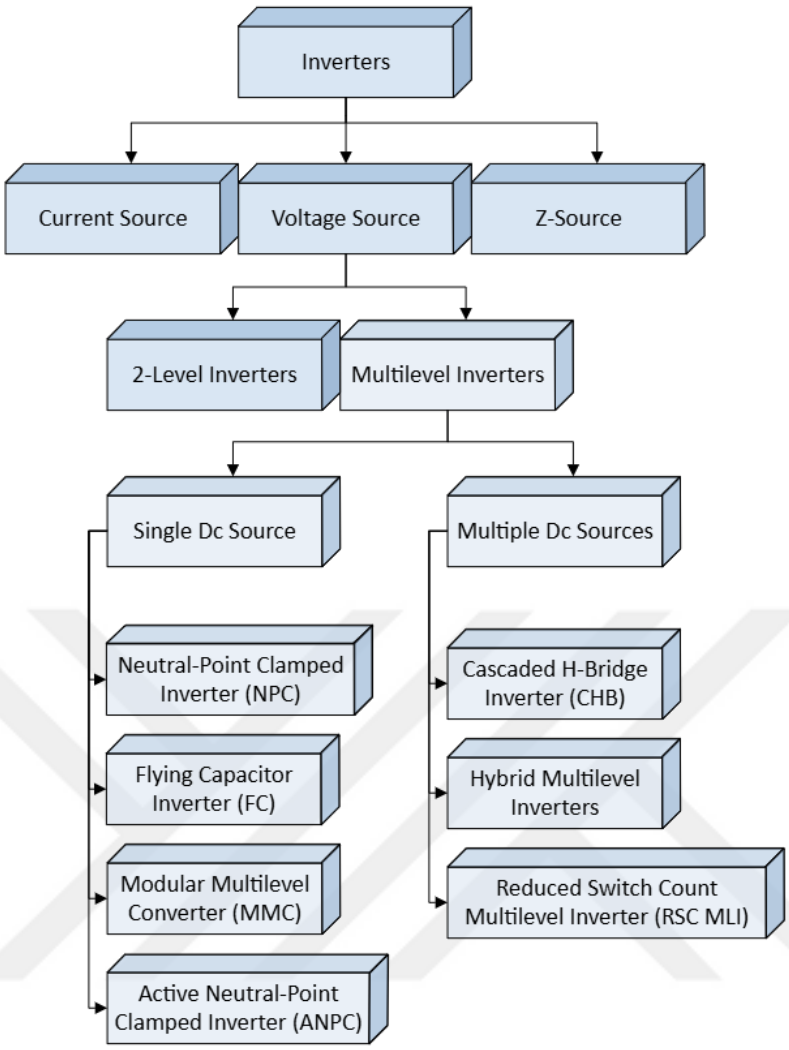


Figure 3.1 Classification diagram of MLIs

The development of MLI architecture has led to the formulation of various topologies, each optimized for specific performance criteria and application domains in power conversion systems. This section presents a detailed review of the most prominent MLI configurations encountered in contemporary literature. The analysis begins with the NPC MLI, which represents a foundational topology known for its effective voltage stress sharing across devices using clamping diodes. Subsequently, the FC MLI is explored, characterized by its phase leg capacitors that facilitate inherent voltage level balancing without the need for complex control schemes. The MMC, widely adopted in high-voltage DC and large-scale grid applications, is then addressed, with emphasis on its modular design, excellent scalability, and low harmonic distortion. Next, the Active Neutral-Point Clamped Inverter is introduced as an enhanced variation of the NPC, capable of better thermal management and current sharing through active switching elements. The

discussion proceeds with the CHB Inverter, notable for its flexibility in achieving high output voltage levels through a series connection of independent H-bridge units, often supplied by isolated DC sources. Moreover, the Hybrid MLI is reviewed, which integrates elements from multiple topologies to optimize specific aspects such as efficiency, voltage level count, or switch utilization. Finally, attention is given to the RSC-MLI, which seeks to minimize the number of power semiconductor devices while still achieving the desired output performance, thereby enabling cost-effective and compact inverter designs suitable for medium- to high-power applications. Each of these topologies will be assessed with regard to their circuit configuration, operational dynamics, merits, drawbacks, and practical use cases [2].

3.2.1 Conventional Topologies

In the literature, three MLI topologies have been widely recognized as conventional configurations due to their historical development, structural maturity, and extensive deployment in industrial and academic applications. Figure 3.2 illustrates the three classical MLI topologies, which are widely recognized in the literature: the NPC (also known as Diode-Clamped MLI), the FC, and the CHB. Each topology exhibits distinct structural features and component requirements, making them suitable for different medium- and high-power applications. In the following sections, these three conventional topologies are examined in detail and comparatively evaluated based on their operational principles and performance characteristics [74].

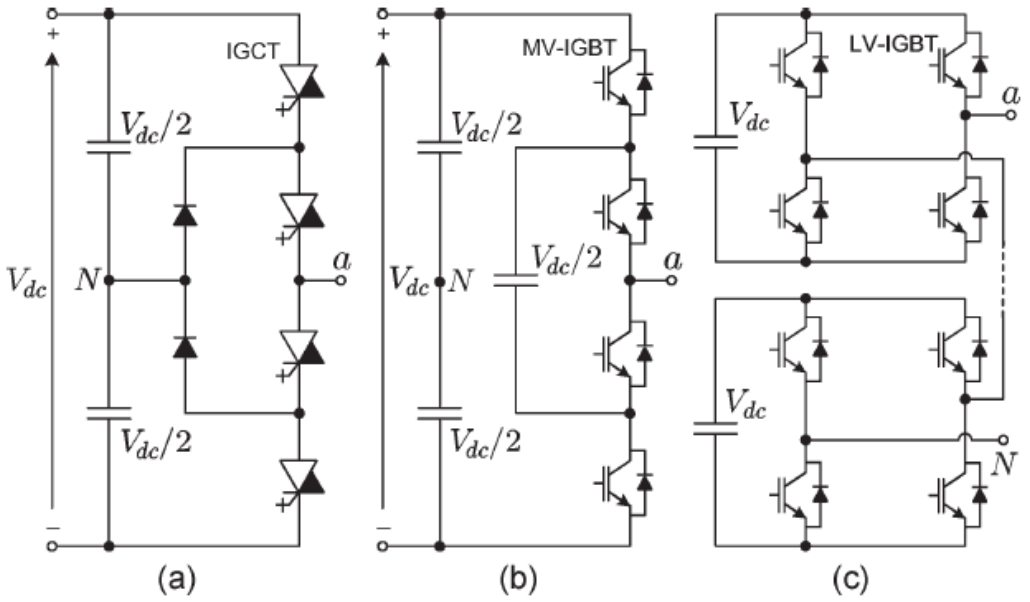


Figure 3.1 Conventional structures of conventional MLI topologies (illustrated for a single phase) are as follows: (a) a three-level NPC configuration utilizing IGCT devices, (b) a three-level FC topology employing medium-voltage IGBTs, and (c) a five-level CHB arrangement based on low-voltage IGBT modules [61]

3.2.1.1 Neutral-Point-Clamped Multilevel Inverter

The NPC MLI represents a foundational MLI topology that enables improved output voltage quality using additional clamping devices. Its circuit configuration incorporates both main switching transistors and auxiliary switching elements, which together clamp the output terminal voltages to the midpoint of the DC bus. This arrangement allows conventional PWM strategies to be effectively applied while achieving reduced harmonic distortion in the output voltage.

Operationally, the NPC inverter modulates switching patterns such that during off-periods, the auxiliary devices maintain the output terminal potential near the neutral point. This results in a reduced voltage swing compared to conventional two-level inverters, thus limiting the harmonic components. An example implementation employing a PWM strategy that eliminates the fifth and seventh harmonics demonstrated superior harmonic performance compared to a conventional topology, as confirmed through both analytical and experimental assessments.

The primary advantages of the NPC topology include decreased harmonic distortion, lower voltage stress across switching devices (halved relative to

conventional inverters), and improved overall drive efficiency. The inverter was shown to achieve approximately 93% system efficiency and a 97% input power factor when driving a standard 2.2 kW induction motor under rated conditions. These characteristics make the NPC inverter suitable for high-efficiency variable-speed motor drive applications.

However, architecture presents several limitations. The use of clamping components increases the number of required switching devices-doubling that of a traditional inverter-thereby raising system complexity and potential thermal management challenges. Furthermore, the current imbalance through clamping paths can arise under certain operating conditions.

In practical terms, NPC inverters are well-suited for medium- to high-power AC motor drive systems requiring low harmonic distortion and efficient voltage control. The modular nature of the design facilitates scalable implementations in industrial drive applications. The article also compares different NPC variants, highlighting that the original NPC structure delivers improved performance over simplified versions and conventional configurations when appropriate PWM strategies are adopted [75].

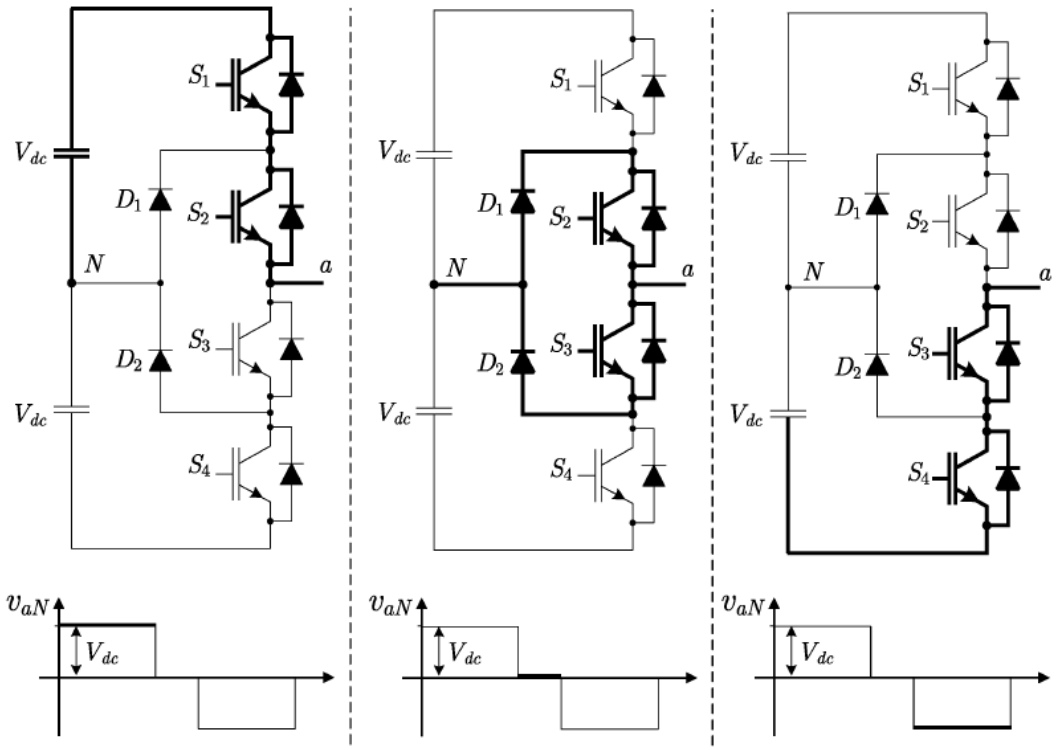


Figure 3.2 Switching configurations and their respective output voltage levels for the three-level NPC inverter [2]

Figure 3.3 illustrates the three distinct switching states of a single phase-leg in a three-level NPC inverter topology and the corresponding output voltage levels at terminal a with respect to the neutral point N.

For positive output level ($V_{aN} = +V_{dc}/2$), switches S_1 and S_2 are turned on, while S_3 and S_4 remain off. Under this condition, the output terminal a is directly connected to the positive rail of the DC bus through the conducting switches, resulting in a positive half of the output voltage.

To obtain the zero-voltage level, switches S_2 and S_3 are turned on, forming a current path through the clamping diodes D_1 or D_2 depending on the current direction. This configuration connects the output terminal a to the neutral point, thereby generating a zero-output voltage.

For negative output level ($V_{aN} = -V_{dc}/2$), switches S_3 and S_4 are turned on, while S_1 and S_2 remain off. The output terminal a is now linked to the negative rail of the DC bus, leading to a negative output voltage level.

In NPC topology, several technical limitations must be addressed to ensure reliable operation. Although each switching device only needs to withstand a voltage of $V_{dc} / (N_{level} - 1)$, the clamping diodes are subjected to higher reverse voltages and therefore require significantly greater voltage ratings. As the number of levels increases, the number of diodes required grows quadratically, making the converter less practical for high-level applications. Furthermore, the unequal conduction times of switching devices lead to non-uniform current stresses, requiring different current ratings and potentially resulting in inefficient sizing- some devices may be over-dimensioned while others are underutilized. Capacitor voltage imbalance is another concern, especially during active power exchange, due to unequal charging and discharging durations. This imbalance typically resolves only under zero power factor conditions, limiting the system's flexibility in varying operational scenarios.

Nevertheless, NPC converters offer noteworthy benefits. When enough voltage levels are implemented, the harmonic distortion of the output waveform is significantly reduced, potentially eliminating the need for bulky output filters. The fact that all switches operate at the fundamental frequency not only improves

efficiency but also reduces EMI. Additionally, reactive power control is feasible, and the control strategy remains relatively simple in back-to-back system configurations. However, as the number of levels increases, the growing number of required clamping diodes adds complexity and cost to the design. Moreover, achieving precise control over real power flow becomes increasingly challenging, which may impact the overall system performance in demanding applications [76].

3.2.1.2 Flying Capacitor Multilevel Inverter

The FC MLI is conceptually represented through the versatile multilevel commutation cell. This topology introduces a modular structure in which the switches are organized into complementary pairs and interconnected with capacitors that do not share a common reference point-hence the term “flying”. The arrangement allows for systematic voltage distribution and supports the generation of multiple output levels from a single DC source. In terms of circuit configuration, each cell comprises two complementary switch pairs, which operate similarly to a standard commutation cell where the switches within a pair must always be in opposite states. Capacitors placed between these pairs establish voltage levels that divide the total DC bus voltage equally. The voltage across each blocking switch remains consistently limited to V_{in} / N_{level}, where V_{in} is the input voltage and N_{level} is the number of levels. This systematic division allows the output voltage to incrementally vary from 0 to V_{in} in steps of V_{in} / N_{level}. From an operational perspective, the FC inverter ensures voltage balancing by maintaining each capacitor’s voltage at fixed values corresponding to their position in the cascade. This balance is essential for consistent multilevel voltage synthesis. Simultaneously, the control strategy must optimize the harmonic spectrum of the output waveform, ensuring reduced distortion without resorting to complex modulation schemes. The topology offers several technical advantages. Chief among them is the uniform voltage stress across switches, which eliminates the need for additional voltage sharing circuits. Furthermore, the fine granularity in voltage levels facilitates improved waveform quality, particularly in terms of harmonic suppression. The modularity of the design also supports ease of scalability for higher voltage applications [77].

Nonetheless, the FC inverter is not without limitations. One of the primary challenges is maintaining capacitor voltage balance, especially under dynamic load

conditions. Moreover, the increased number of components - specifically switches and capacitors - adds to the overall system complexity, size, and potential cost. Despite these challenges, the FC inverter configuration is highly suited for high-voltage applications where conventional semiconductor devices fall short in voltage handling capabilities. Its inherent ability to achieve better waveform quality and controlled voltage stress makes it applicable in systems such as high-voltage choppers and voltage-source inverters, particularly in contexts where harmonic performance is critical [64].

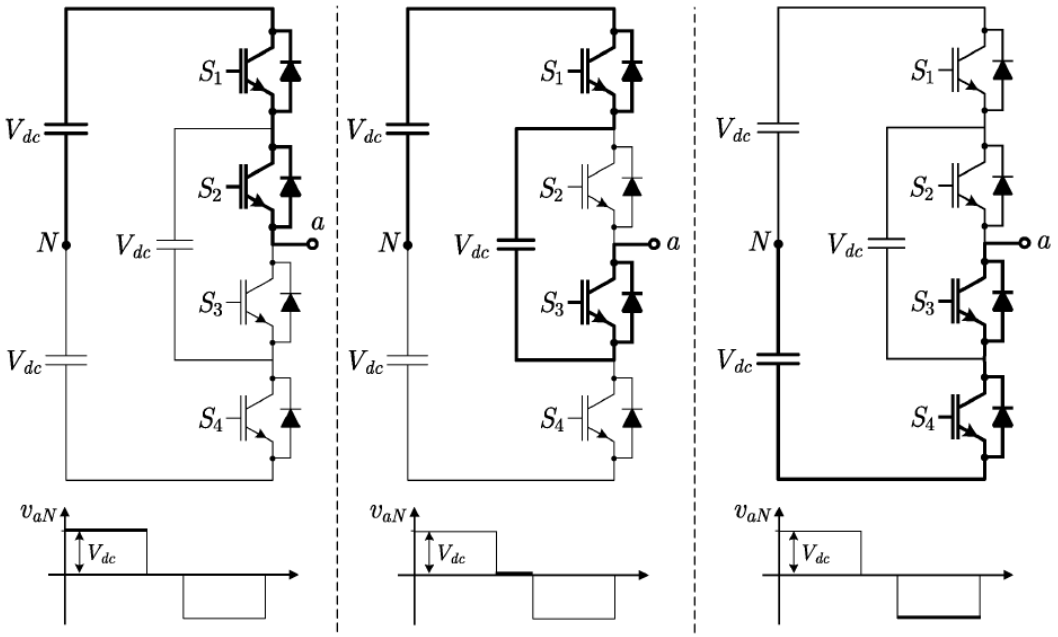


Figure 3.3 Switching configurations and their respective output voltage levels for the three-level FC inverter [2]

Figure 3.4 illustrates the three distinct switching states of a single-phase leg in a three-level FC inverter topology and the corresponding output voltage levels at terminal “a” with respect to the neutral point N.

For the positive output voltage level ($V_{aN} = +V_{dc}$), switches S_1, and S_2 are turned on, while S_3 and S_4 remains off. Under this configuration, the output terminal a is directly connected to the positive rail of the DC bus through the conducting switches, resulting in a positive output voltage. The FC simultaneously enters the charging state.

To obtain the zero-output voltage level ($V_{aN} = 0$), switches S_2 and S_3 are turned on, while S_1 and S_4 are kept off. This switching pattern causes the output terminal “a”

to connect across the FC, producing a zero-voltage level while allowing the capacitor to either charge or discharge depending on the load current direction.

For the negative output voltage level ($V_{aN} = -V_{dc}$), switches S_3, and S_4 are turned on, and switch S_1, and S_2 are turned off. This connects the output terminal to the negative rail of the DC bus, producing a negative output voltage. The switching condition also facilitates balancing of the FC voltage through controlled charging or discharging.

In addition to the challenge of maintaining capacitor voltage balance during real power conversion, the FC topology faces a major limitation due to its significant reliance on energy storage elements. Assuming each capacitor has the same voltage rating as the main power switch, an N_{level}-level inverter requires (N_{level} - 1) main DC bus capacitors per phase leg, along with (N_{level} - 1) × (N_{level} - 2) / 2 auxiliary capacitors. In contrast, a NPC inverter with the same voltage assumptions only requires (N_{level} - 1) capacitors. To ensure charge-balancing among capacitors, multiple switching combinations must be applied at intermediate voltage levels over one or more fundamental cycles. While this approach enables real power conversion with proper switching patterns, it introduces considerable complexity into the selection process and necessitates a switching frequency higher than the fundamental one.

Despite these drawbacks, the FC converter topology offers several notable advantages. The abundance of storage capacitors allows the system to maintain operation momentarily during power outages, enhancing its ride-through capability. Additionally, the redundancy in switching combinations helps balance voltage levels more effectively. With a sufficiently high number of levels, the harmonic distortion of the output is greatly reduced, potentially eliminating the need for output filters. Since the FC inverter can handle both active and reactive power flow, it stands as a viable VSC candidate for HVDC transmission applications. Nevertheless, the excessive number and volume of capacitors required in high-level designs increase system cost and packaging complexity. Moreover, for real power transmission, the control strategy becomes highly intricate, and higher switching frequencies lead to increased switching losses-posing critical limitations to the practical deployment of this topology [76].

3.2.1.3 Cascaded H-Bridge Multilevel Inverter

The CHB MLI topology is composed of multiple single-phase full bridge inverter units connected in series, each powered by an isolated DC source. Designed to meet the demands of high-voltage and high-power applications, this structure enables efficient energy conversion while offering modular architecture and reduced harmonic distortion. CHB inverters have been widely adopted in applications such as static var generators, power-line voltage balancing, series compensation, and PV system interfaces due to their operational versatility and scalability. In terms of construction, the CHB inverter employs (N_{level} - 1) / 2 full-bridge inverters to generate an N_{level} -level output. For instance, achieving an 11-level output requires five independent full bridge inverter units. Each unit, powered by its own isolated DC source, contributes discrete voltage levels of $+V_{dc}$, 0, or $-V_{dc}$, which combine to synthesize a staircase-like output waveform. This design eliminates the need for bulky transformers, clamping diodes, and flying capacitors typically found in conventional MLI configurations, thereby reducing system complexity and physical volume. Operation of the CHB inverter relies on independent controlling each full bridge inverter unit through predefined switching angles. These angles are carefully selected to minimize THD in the output while simultaneously allowing the DC-link capacitors to self-balance their voltages during normal operation. The flexibility of the topology extends to three-phase applications as well, where multiple CHB modules can be configured in star or delta connections, enabling broader system integration without major structural alterations.

One of the key advantages of the CHB topology lies in its significantly lower component count. For example, while a traditional 51-level inverter may require over 7,000 clamping diodes, the CHB structure operates without any. Additionally, by removing the necessity for transformers-which often constitute nearly 40% of the total system volume-CHB inverters achieve a compact and efficient layout. Experimental results have demonstrated system efficiencies as high as 93%, and the modular nature of the design allows for straightforward scalability up to at least 21 voltage levels. The effectiveness of the CHB inverter has been substantiated through both experimental and simulation-based validations. A prototype static var generator rated at ±1 kVAr confirmed its practical viability, while simulations of a 21-level CHB inverter successfully interfaced with a 13 kV utility grid, maintaining

DC voltage ripple below 5%. These performance indicators affirm the CHB inverter's suitability for advanced power electronics applications, including FACTS devices, renewable energy systems, and high-efficiency AC power conversion interfaces.

In conclusion, the CHB inverter stands out as a modern and robust solution that addresses many of the limitations associated with earlier MLI designs. Its modularity reduced harmonic output, minimal control complexity, and proven high-efficiency performance make it an ideal candidate for demanding power conversion tasks across a wide range of industrial and renewable energy applications [77].

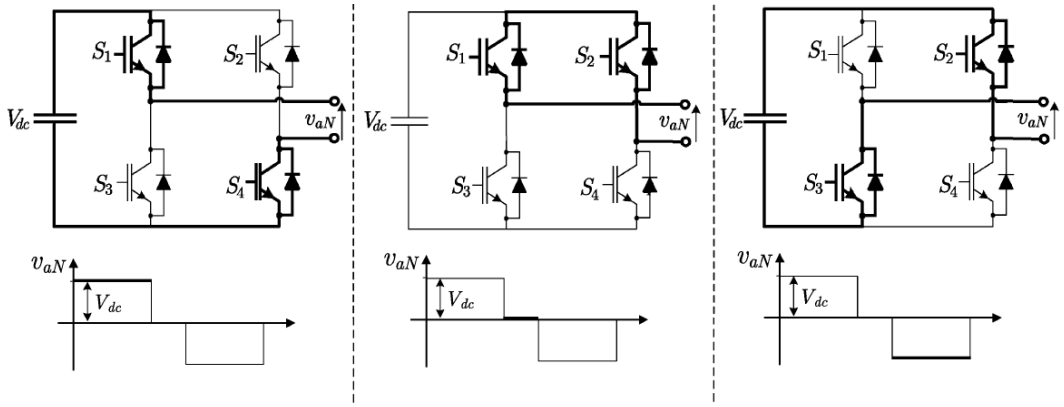


Figure 3.4 Switching configurations and corresponding output voltage levels in a single-phase three-level H-bridge inverter [2]

Figure 3.5 illustrates the switching configurations and corresponding output voltage levels in a single-phase three-level H-bridge inverter.

For the positive output voltage level ($V_{aN} = + V_{dc}$), switches S_1 and S_4 are turned on, while S_2 and S_3 remain off. In this state, the load is connected to the positive terminal of the DC source, producing a positive output voltage at terminal a.

To achieve the zero-voltage level ($V_{aN} = 0$), either switch pair S_1-S_2 or S_3-S_4 is turned on simultaneously, effectively circuiting the output terminals and resulting in zero voltage across the load.

For the negative output voltage level ($V_{aN} = -V_{dc}$), switches S_2 and S_3 are turned on, while S_1 and S_4 remain off. This connects the load to the negative terminal of the DC source, generating a negative output voltage at terminal a.

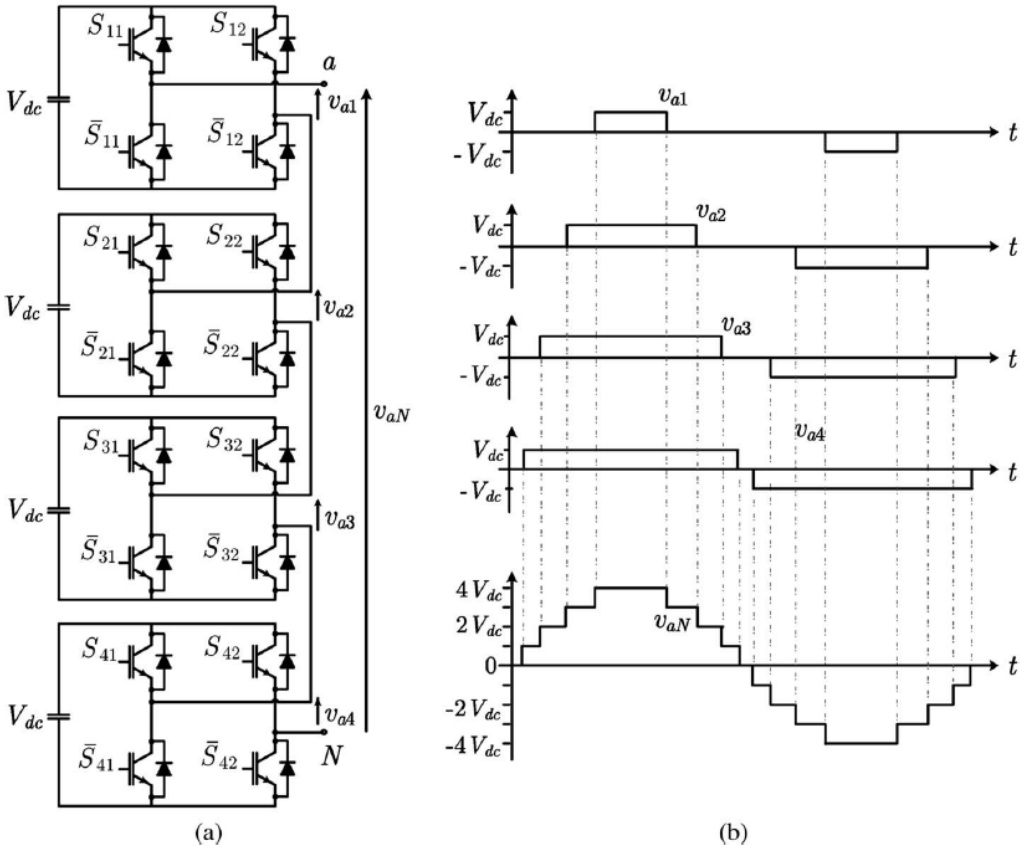


Figure 3.5 Single-phase nine-level CHB inverter: (a) circuit configuration and (b) synthesized output voltage waveform [2]

When multiple H-bridge cells are connected in series, their individual output voltages are algebraically summed to generate multiple voltage levels, thereby enhancing the total output voltage and power capacity of the inverter. Figure 3.6 illustrates a configuration comprising four CHBs and an example of their respective three-level output voltages. The resulting output waveform exhibits nine distinct voltage levels. In general, connecting $N_{h\text{-}bridge}$ H-bridge modules in series yields 2 x $N_{h\text{-}bridge}$ + 1 voltage levels - including two levels per H-bridge and a common zero level - and enables a maximum output voltage of $N_{h\text{-}bridge}$ x V_{dc}.

The CHB MLI topology requires isolated DC sources for each individual module. This architecture is particularly well-suited for distributed renewable energy applications, such as fuel cells, PV panels, and biomass systems, where separate energy sources can be individually connected to the corresponding H-bridge cells. However, connecting two such converters in a back-to-back configuration introduces the risk of a short circuit if the switching operations are not perfectly synchronized, making such arrangements impractical without precise control. The

inherent modularity of the CHB structure, where each level has an identical circuit layout, facilitates a simplified and scalable system design without the need for additional clamping diodes or voltage balancing capacitors.

Among the various MLI topologies, the CHB requires the fewest components to achieve a given number of output voltage levels. Its uniform cell structure enhances modularization and makes the circuit packaging straightforward. Furthermore, soft-switching techniques can be employed within this topology to minimize the reliance on bulky and lossy resistor-capacitor-diode snubbers, improving overall efficiency. Nevertheless, the primary limitation lies in the necessity for independent DC sources, which restricts their applicability in centralized power conversion systems. This requirement may complicate implementation in large-scale utility or industrial power infrastructures where such isolated sources are not readily available [76].

3.2.2 Active Neutral-Point-Clamped Multilevel Inverter

The ANPC MLI topology was introduced to overcome key drawbacks observed in traditional NPC designs. This topology comprises two DC-link capacitors connected in series, primary switching devices for current conduction, and additional active clamping switches used for regulating the neutral point potential. Unlike the conventional NPC, where fixed diodes are used for clamping, ANPC uses actively controlled switches, enabling more flexible current and voltage path configurations. This architectural improvement enhances both control capability and voltage balancing performance. Figure 3.7 illustrates the three-phase configuration of the ANPC topology [78].

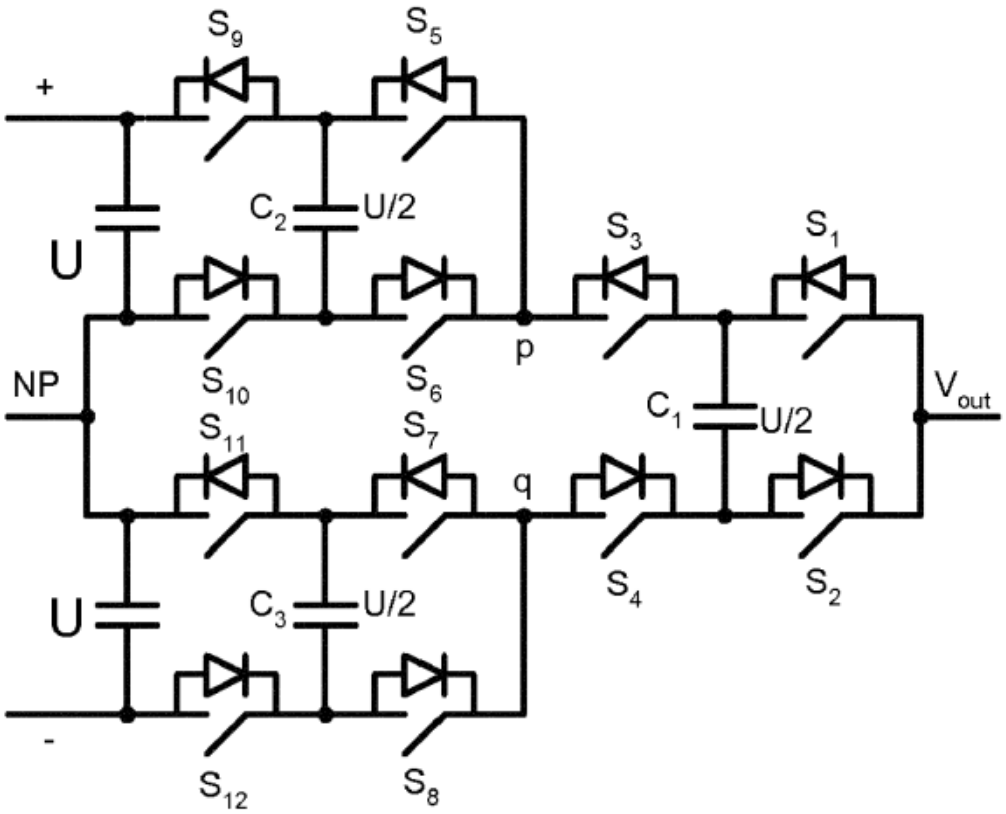


Figure 3.1 The ANPC VSC configured in a three-level topology [78]

From an operational standpoint, ANPC allows dynamic alteration of current paths during switching events, thus distributing conduction losses more evenly among the devices and preventing overloading of specific switches. The neutral-point voltage is actively regulated, resulting in more balanced voltage division across the DC-link capacitors. This not only improves the quality of the output waveform but also reduces harmonic distortion. One of the most notable advantages of the ANPC topology is improved thermal management. Since the current can be routed through different switches, the thermal load is more evenly distributed, minimizing temperature gradients between semiconductor devices and extending their operational lifespan. Furthermore, reduced common-mode voltage leads to lower EMI and eases insulation demands on connected loads. The topology also enables wider modulation index ranges due to the flexibility of active switching, allowing high-quality voltage waveforms even at relatively low switching frequencies. On the downside, the ANPC design introduces additional complexity in both hardware and control. Active clamping switches require separate gate drivers, and the control system must implement sophisticated algorithms to maintain stable neutral-point

voltage. High precision in timing and synchronization is necessary, which in turn increases the burden on protection and control circuits [78].

Despite its performance advantages, the ANPC topology introduces notable design and control complexities. The inclusion of active clamping switches necessitates additional gate drivers, while the hybrid nature demands meticulous coordination of switching states across devices operating at significantly different frequencies. Moreover, effective neutral-point voltage regulation requires precise feedback mechanisms and advanced modulation strategies such as level-shifted PWM. The system must also address the risk of shoot-through faults, particularly due to the high-speed switching behaviour of wide band gap devices, which calls for split inductor design and transient suppression circuits. These factors collectively increase the computational and hardware burden on the controller, requiring enhanced synchronization, protection logic, and EMI mitigation measures to ensure reliable operation under varying load conditions [79].

3.2.3 Modular Multilevel Converter

The MMC represents a significant advancement in power electronics, particularly for medium to high-voltage applications. It consists of multiple submodules per phase arm, typically built using half-bridge or full-bridge cells, which are connected in series to form a scalable and modular structure (see Figure 3.8). Each submodule contains its own capacitor and switching devices, enabling the generation of multistep output voltages with reduced harmonic distortion.

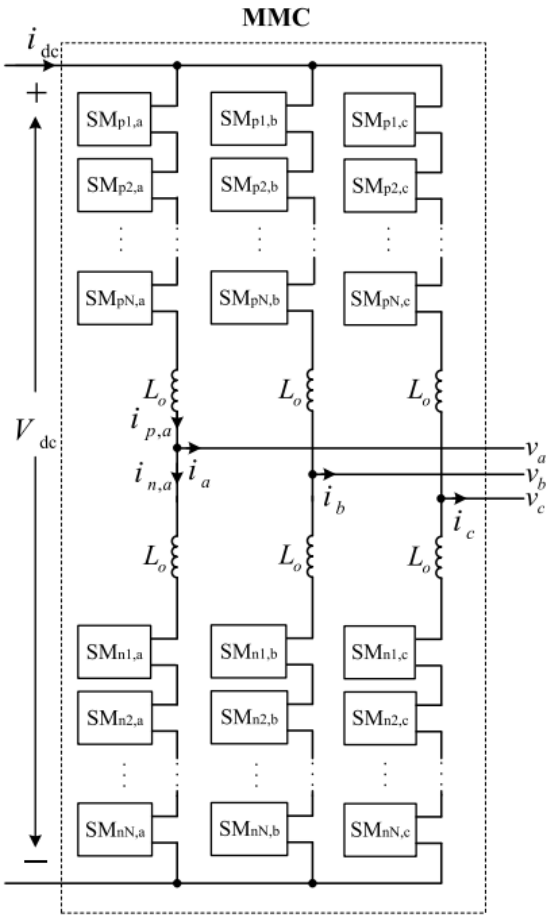
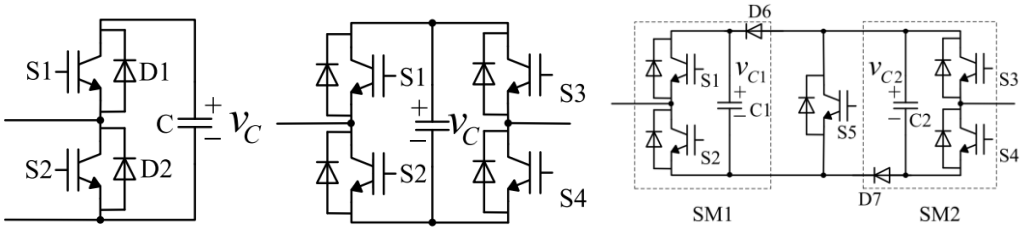
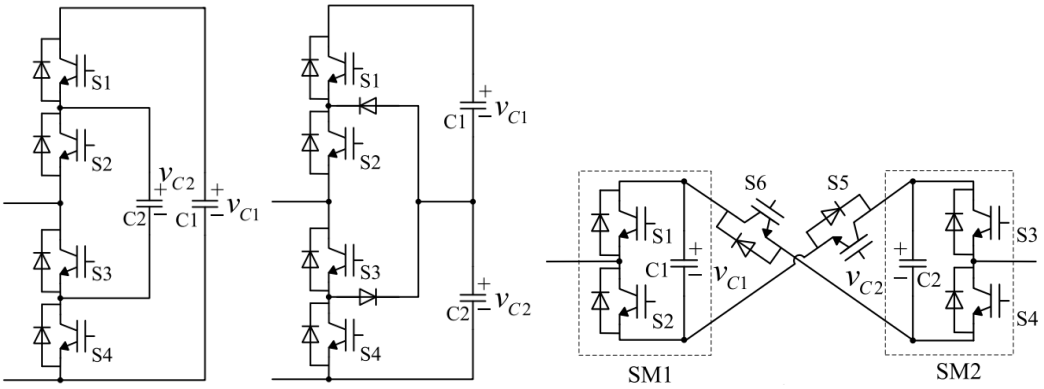


Figure 3.1 Illustrative schematic of the MMC topology [68]

From an operational standpoint, MMCs function by balancing the capacitor voltages of individual submodules (see Figure 3.9) while ensuring continuous current flow through both the AC and DC sides. This is achieved through sophisticated control algorithms that manage submodule insertion and bypass operations dynamically. The result is a near-sinusoidal output waveform with high power quality, minimal filter requirements, and improved electromagnetic compatibility [80].



(a) (b) (c)



(d) (e) (f)

Figure 3.2 Different submodule configurations include: (a) half-bridge, (b) full-bridge, (c) clamped-double, (d) three-level FC, (e) three-level NPC, and (f) five-level cross-connected submodule structures [80]

Among the key merits of the MMC topology are its modular scalability, fault tolerance, and the ability to handle high voltage and current ratings without requiring bulky transformers or external clamping circuits. Moreover, its distributed energy storage within submodules enhances reliability and allows for redundancy. However, MMCs also face several challenges. The need for precise capacitor voltage balancing, complex control schemes, and increased component count can lead to higher initial design and operational complexity. Additionally, submodule communication and synchronization are critical for stable operation, particularly in large-scale implementations. MMC technology has found practical applications in HVDC transmission systems, FACTS, motor drives, and renewable energy integration. Its ability to interface efficiently between AC and DC networks makes it a core technology in the future of smart grids and energy infrastructure [81].

3.2.4 Hybrid Multilevel Inverters

Hybrid MLIs represent a strategic approach to enhancing output waveform quality and improving overall performance metrics. These inverters are constructed by integrating two distinct MLI topologies, leveraging the flexibility provided by the proportional relationship between multiple DC voltage levels. Various hybrid configurations have been proposed in the literature, often categorized by their design methodology. The primary methods for developing hybrid MLIs include: (i) combining conventional topologies such as NPC MLI with CHB MLI or FC MLI

with CHB MLI; (ii) merging two RSC-MLI topologies; and (iii) integrating a reduced-switch-count topology with a traditional MLI structure. These combinations exploit topological synergy to reduce component count while maintaining or improving power quality and modulation capability. The following studies present representative hybrid MLI topologies that correspond to the three main design approaches outlined above [82].

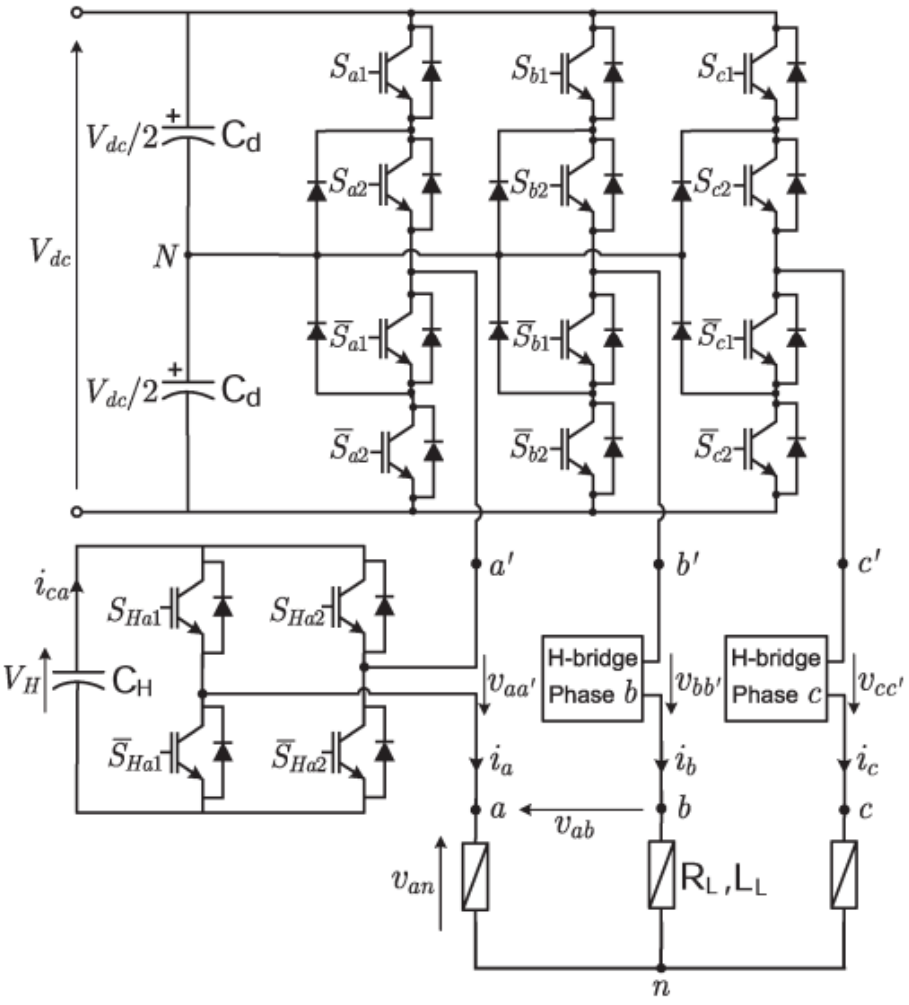


Figure 3.1 Power circuit of the hybrid MLI topology [83]

In [83], the authors present a hybrid MLI composed of a three-level NPC converter in series with floating H-bridge cells, aiming to improve output current waveform quality in medium-voltage applications (see Figure 3.10 for the hybrid inverter topology). The NPC stage, modulated using SHE at low switching frequency, handles the active power, while the H-bridges function as series active filters, injecting reactive power to compensate harmonic distortions. A floating DC-link

voltage control strategy enables the H-bridges to operate without external power sources, maintaining stable capacitor voltages via a dual-reference modulation scheme. Experimental validation with a 1 kW prototype demonstrates that the hybrid configuration significantly reduces THD, achieving a current THD as low as 2.4% compared to 12.9% in conventional NPC-only operation. This architecture provides a compact and efficient alternative to bulky LCL filters, enhancing power quality without increasing the converter's power rating [83].

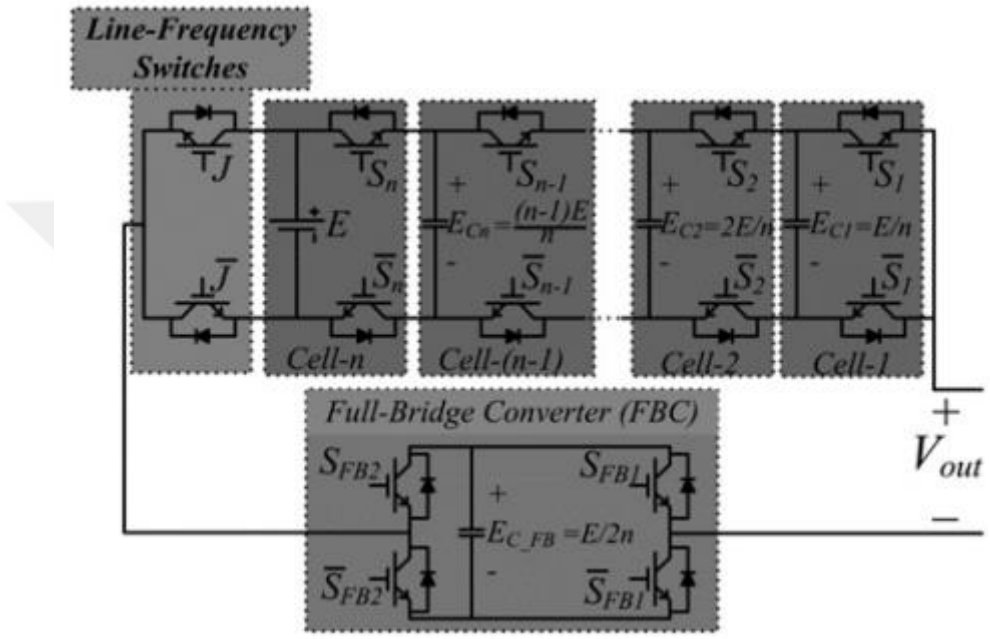


Figure 3.2 Hybrid double flying capacitor multicell (DFCM) MLI topology [84]

In [84], the authors introduced an innovative hybrid MLI topology designed for grid-connected renewable energy systems, achieved by cascading a DFCM MLI with a full-bridge converter that incorporates a floating capacitor (see Figure 3.11 for the hybrid DFCM topology). The architecture effectively enhances output voltage levels while reducing the number of flying capacitors and power switches, thereby improving efficiency and lowering cost. A distinctive feature of the proposed system is its ability to achieve natural voltage balancing for both flying and floating capacitors through a tailored switching and modulation scheme, eliminating the need for voltage sensors or feedback control. Simulation and experimental evaluations confirm the converter's capability to inject and absorb active and reactive power, ensuring stable operation and compliance with grid standards under varying power demands [84].

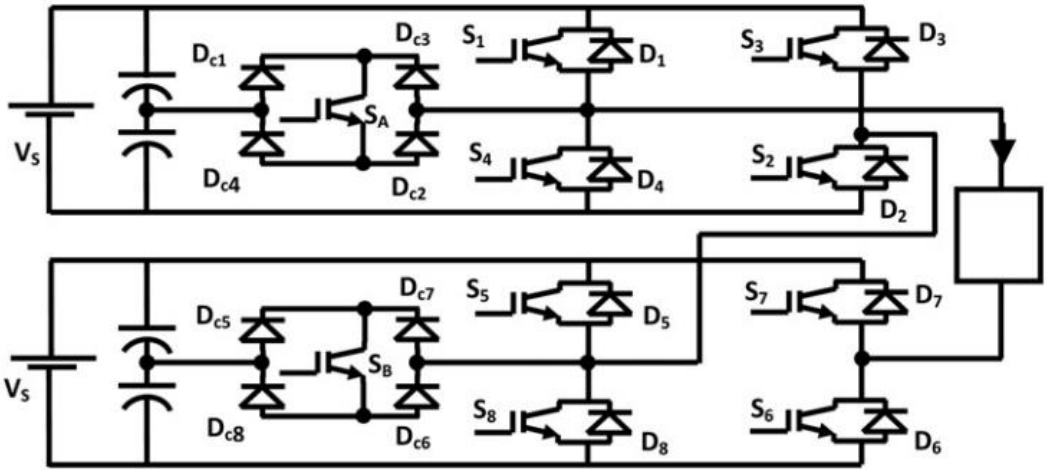


Figure 3.3 9-level cascaded MLI topology [85]

In [85], the authors proposed a single-phase 9-level hybrid cascaded MLI topology, formed by connecting two modified five-level inverter units in series (as illustrated in Figure 3.12). Each unit integrates a conventional full-bridge H-bridge, and an auxiliary bidirectional switch placed between two DC sources, enabling nine distinct voltage levels through a multicarrier phase disposition PWM scheme. The inverter is capable of synthesizing 3-, 5-, 7-, and 9-level waveforms depending on the modulation index, offering flexibility in control. Both simulation and experimental results from a 2.12 kW prototype confirm the feasibility of the design, with a measured THD of 10.12% at a modulation index of 0.8. Compared to conventional 9-level inverters, the proposed topology achieves a lower component count and improved harmonic performance, making it suitable for compact single-phase applications [85].

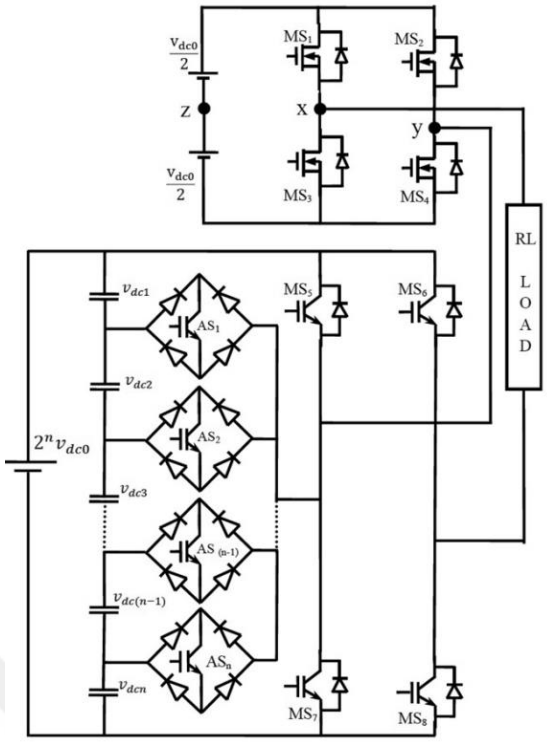


Figure 3.4 Hybrid MLI based on a CHB structure [86]

In [86], the authors introduced a generalized single-phase hybrid CHB MLI topology with reduced switch count and isolated DC sources (as shown in Figure 3.13). The proposed structure consists of two H-bridge inverters connected in cascade: the upper inverter produces a two-level output at high switching frequency, while the lower inverter, aided by an auxiliary circuit of diodes and switches, generates multiple voltage levels at low frequency. A unique feature of the topology is its scalability, where each added switch in the lower bridge increases the number of levels by four. The authors also proposed a general modulation algorithm to control any number of voltage levels using simple logical and arithmetic operations. Simulation and experimental results for up to 43 levels validated the proposed scheme's effectiveness in reducing THD, conduction, and switching losses, while achieving flexible control through modulation index adjustment [86].

3.2.5 Reduced Switch Count Multilevel Inverters

RSC-MLIs have gained significant attention due to their ability to minimize the number of power semiconductor devices while maintaining acceptable output quality and system performance. These topologies are particularly advantageous in

cost-sensitive and space-constrained applications, as they aim to achieve higher voltage levels with fewer components.

In the literature, RSC-MLI configurations are generally categorized based on symmetry and the presence of H-bridge structures. Accordingly, the following subsections provide a detailed classification and analysis of RSC-MLIs under four main groups: (i) asymmetrical topologies with H-bridge, (ii) symmetrical topologies with H-bridge, (iii) asymmetrical topologies without H-bridge, and (iv) symmetrical topologies without H-bridge [87].

Each study is systematically examined in terms of (i) design motivations, (ii) proposed topologies and operating principles, (iii) modulation or control strategies employed, (iv) targeted application domains, (v) reported advantages and limitations, and (vi) specific contributions to the existing body of knowledge. This structured approach provides a comprehensive understanding of the current landscape of RSC-MLI research and its relevance to contemporary power electronic systems.

3.2.5.1 Asymmetrical Reduced Switch Count Topologies With H-bridge

Asymmetrical RSC-MLI topologies based on H-bridge structures aim to increase the number of output voltage levels while minimizing hardware complexity and cost. Compared to conventional multilevel designs, these topologies employ fewer switching devices, which enhances system efficiency and simplifies the gate driver circuitry. By utilizing asymmetrical DC voltage ratios, they can achieve a higher number of output levels with reduced harmonic distortion. The literature presents numerous configurations following this design philosophy, generally evaluated in terms of component minimization, modularity, harmonic performance, and control simplicity. In this context, asymmetrical H-bridge-based RSC-MLI topologies provide promising solutions for applications requiring high efficiency and hardware-level optimization.

In the following sections, the relevant studies on these topologies are comprehensively analyzed in terms of their design motivations, structural configurations, operating principles, modulation and control strategies, application areas, advantages and limitations, and contributions to literature.

The MLDCL inverter proposed by Su (2005) addresses the challenge of excessive component count in conventional MLIs, such as NPC, FC, and CHB topologies, which require 2 x (N_{level} - 1) active switches. The design motivation centers on reducing switch count, gate drivers, clamping diodes, and capacitors while maintaining voltage waveform quality. The cascaded half-bridge MLDCL variant employs (2 x N_{dc} + 4) switches and N_{dc} independent DC sources, classified as asymmetrical topology due to discrete voltage sources, integrated with a single-phase full-bridge inverter. The operating principle synthesizes a staircase DC-link voltage via cascaded half-bridge cells, which toggle between bypass and active states at twice the fundamental frequency, while the H-bridge inverts polarity at the fundamental frequency. Modulation involves selective switching of half-bridge cells with duty-cycle control to balance DC-source utilization, facilitated by a DSP-based gate driver (TMS320F240). The topology targets low-power applications (<100 kW), such as permanent-magnet motor drives with low inductance, and high-voltage systems using IGBTs/GTOs. Key advantages include a 50% reduction in switches compared to conventional MLIs, zero-voltage switching for H-bridge devices, and experimental validation of <1% current THD. Limitations include voltage-balancing challenges in NPC configurations without back-to-back operation. The cascaded half-bridge structure is modular, scalable to higher levels by adding cells, whereas NPC and FC versions exhibit fixed modularity. Su's work contributes experimentally validated efficiency, demonstrating a 13-level prototype with 1% THD and reduced component count, establishing MLDCL as a hardware-efficient alternative for RSC-MLI applications [3].

Hinago and Koizumi (2010) propose a single-phase MLI topology, referred to as the Switched Series/Parallel Sources inverter, that addresses the escalating switch count in conventional CHB and switched-capacitor inverters-particularly critical for EV and renewable energy applications where hardware complexity and harmonic distortion are limiting factors. The design aims to minimize active switches and gate drivers while enhancing waveform quality through switched series/parallel reconfiguration of DC voltage sources. The topology employs an asymmetrical H-bridge structure with discrete DC sources and utilizes 11 switches for an 11-level output (vs. 12 in CHB) or 14 switches for 15 levels (vs. 16 in CHB). Voltage synthesis occurs via series/parallel switching of DC sources using switches,

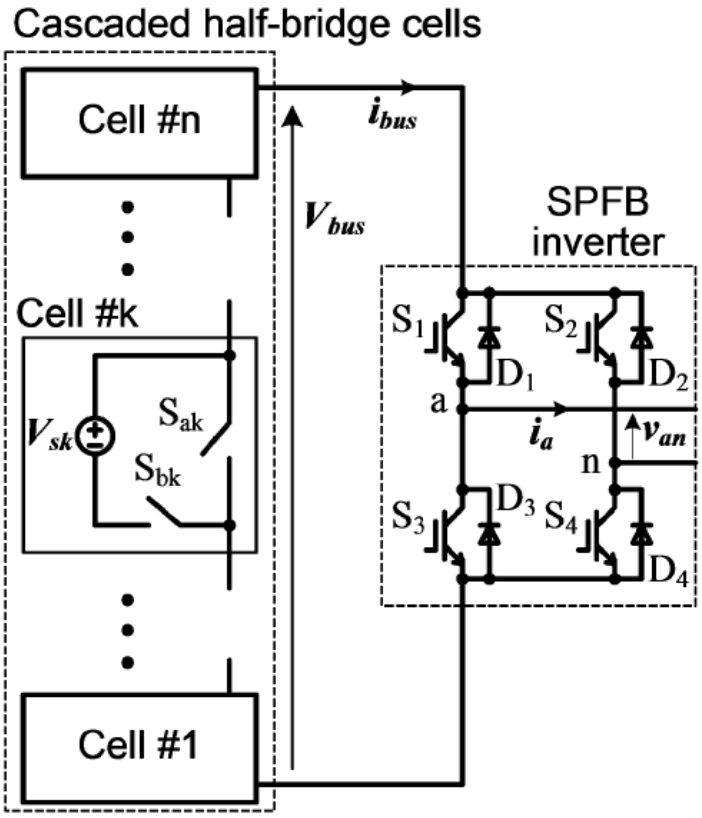
combined with an H-bridge that inverts polarity at the fundamental frequency. A hybrid modulation strategy integrates low-frequency switching for high-voltage devices and high-frequency PWM for low-voltage devices, managed via FPGA-based control. The inverter targets medium-to-high-power domains, including EVs and grid-tied PV systems, where reduced THD (14.6% experimentally) and component count are advantageous. Key strengths include a 50% reduction in switches compared to SC inverters (11 vs. 28 for 11 levels), modular scalability by adjusting DC source ratios, and optimized device selection. Limitations include dependency on precise DC source voltage ratios and challenges in bidirectional power flow without diode replacements. Comparative analysis highlights superior efficiency (92.4% experimental) and lower switch count versus CHB and SC counterparts. The authors validate the topology through MATLAB simulations and a prototype, demonstrating alignment between theoretical and experimental THD (14.6%) and output waveforms. This work contributes a hardware-efficient, modular RSC-MLI solution, validated for practical applications requiring harmonic suppression and reduced component overhead [11].

Babaei et al. (2014) propose a cascaded MLI topology, known as Hexagonal Switched Cell, to address the challenges of component count reduction and modularity in high-voltage applications, emphasizing scalability and cost efficiency. The design aims to minimize switches, diodes, driver circuits, and DC sources while reducing blocked voltage stress on switches. The topology employs 6n unidirectional switches and 2n asymmetrical DC sources per n series-connected H-bridge units, structured as cascaded "developed H-bridge" modules. Each unit synthesizes seven voltage levels via complementary switching states, avoiding simultaneous activation of leg switches to prevent source short-circuiting. A 49-level prototype is developed by cascading two inverter units powered by four distinct DC voltage sources rated at 10 V, 20 V, 70 V, and 140 V, producing output levels reaching up to 240 V. The topology targets renewable energy integration, FACTS devices, and motor drives requiring isolated DC sources. Key advantages include a 50% reduction in IGBTs compared to conventional CHB MLIs (e.g., 12 vs. 24 switches for 49-level), lower blocked voltage, and modular scalability. Limitations include dependency on isolated DC sources and higher source variety in asymmetric configurations. Comparative analysis demonstrates enhanced

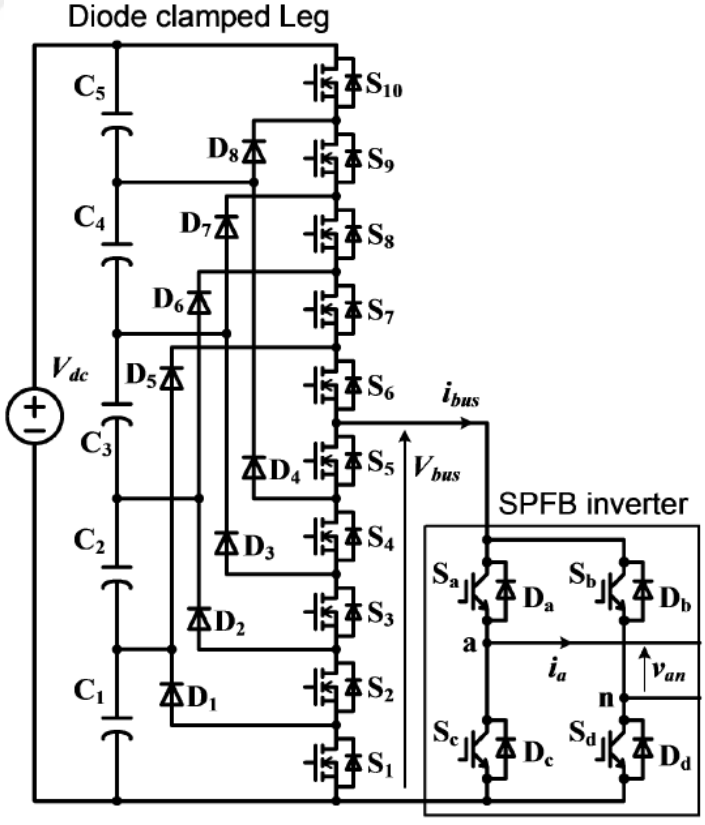
performance, as validated through a 49-level experimental setup under a resistive-inductive load consisting of a 100-ohm resistor and a 55-millihenry inductor. The results confirm that the current exhibits a THD as low as 0.1 percent, with unidirectional power switches operating within a blocking voltage range from 10 volts to 240 volts. This work advances RSC-MLI research by demonstrating a scalable, component-efficient architecture with validated experimental performance, balancing cost and waveform quality for high-power systems [21].

Prabaharan et al. (2020) introduce a trinary sequence-based MLI topology to address the challenge of achieving high output voltage levels with minimal components while ensuring full additive/subtractive DC source combinations. The design aims to minimize switch and DC source counts through a trinary progression (1:3 ratio), enabling a 9-level output with only nine switches (four active devices per level) and two asymmetrical DC sources. The topology combines a level generation unit for positive voltage synthesis and an H-bridge polarity reversal unit, avoiding simultaneous activation of complementary switches to prevent short circuits. Operating modes generate ±60 V, ±120 V, ±180 V, ±240 V, and zero levels. A unipolar phase-disposition PWM scheme reduces the number of carrier signals by half compared to bipolar modulation techniques. In this method, some of the power switches operate at a switching frequency of 5 kHz, while others are operated only at the fundamental frequency to minimize switching losses. The topology targets renewable energy systems, FACTS devices, and medium-voltage drives requiring isolated DC sources. Advantages include a 50% switch reduction versus CHB (e.g., 9 vs. 12-16 switches for 9-level), lower driver count, and modular scalability. Limitations include dependency on isolated DC sources and high voltage stress on H-bridge switches, mitigated using IGCTs. This work advances RSC-MLI research by validating trinary-sequence architecture with reduced component counts, novel asymptotic THD calculation, and experimental verification of 240 V output, balancing efficiency and waveform quality for high-power applications [33].

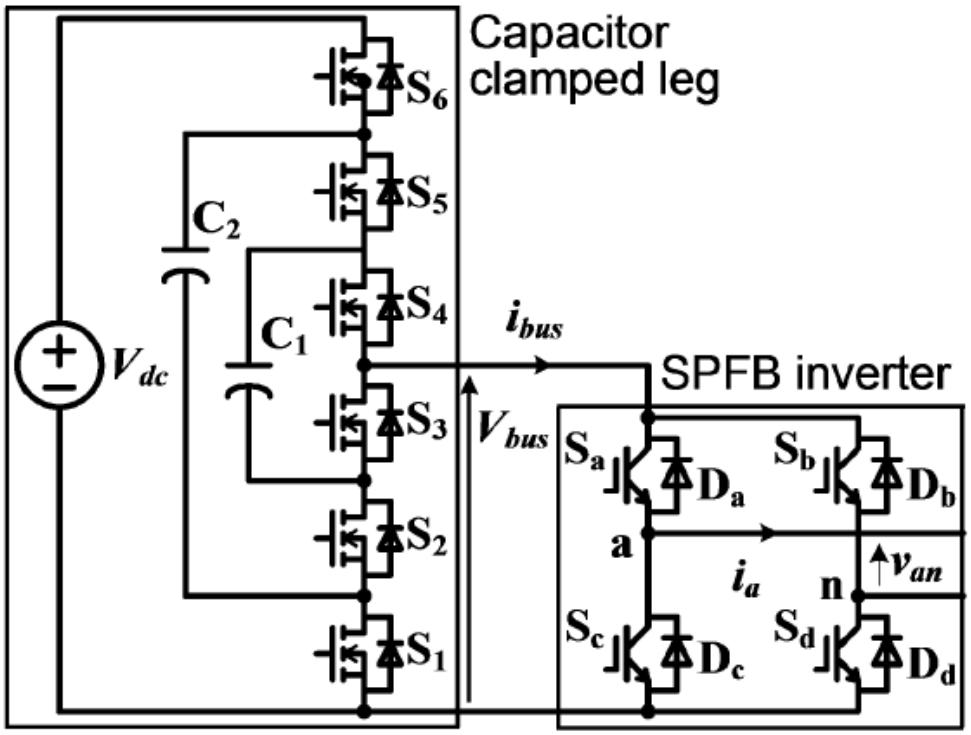
The "Asymmetrical Reduced Switch Count Topologies With H-bridge" discussed above are illustrated in Figure 3.14.


Cascaded half-bridge cells
Cell #n
Cell #k
Cell #1
i_{bus}
V_{bus}
SPFB inverter
S_1
S_2
D_1
D_2
a
i_a
v_{an}
n
S_3
D_3
S_4
D_4
V_{sk}
S_{ak}
S_{bk}

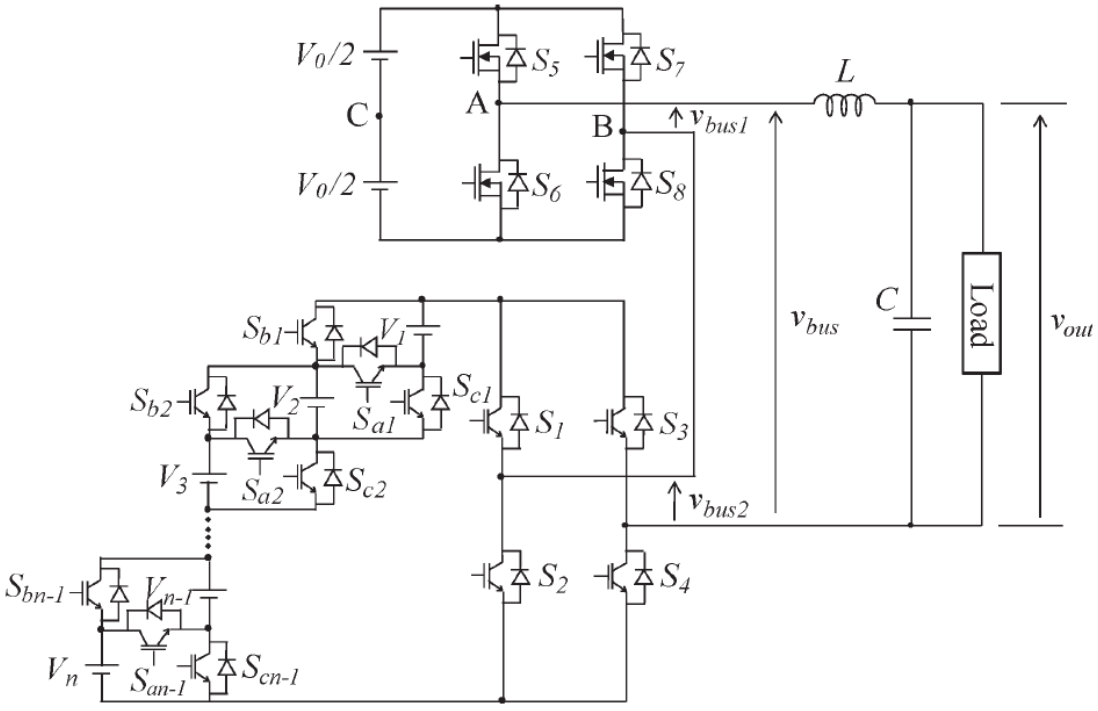
(a)


Diode clamped Leg
C_5
C_4
C_3
C_2
C_1
V_{dc}
S_{10}
S_9
S_8
S_7
S_6
S_5
S_4
S_3
S_2
S_1
D_8
D_7
D_6
D_5
D_4
D_3
D_2
D_1
i_{bus}
V_{bus}
SPFB inverter
S_a
S_b
D_a
D_b
a
i_a
v_{an}
n
S_c
S_d
D_c
D_d

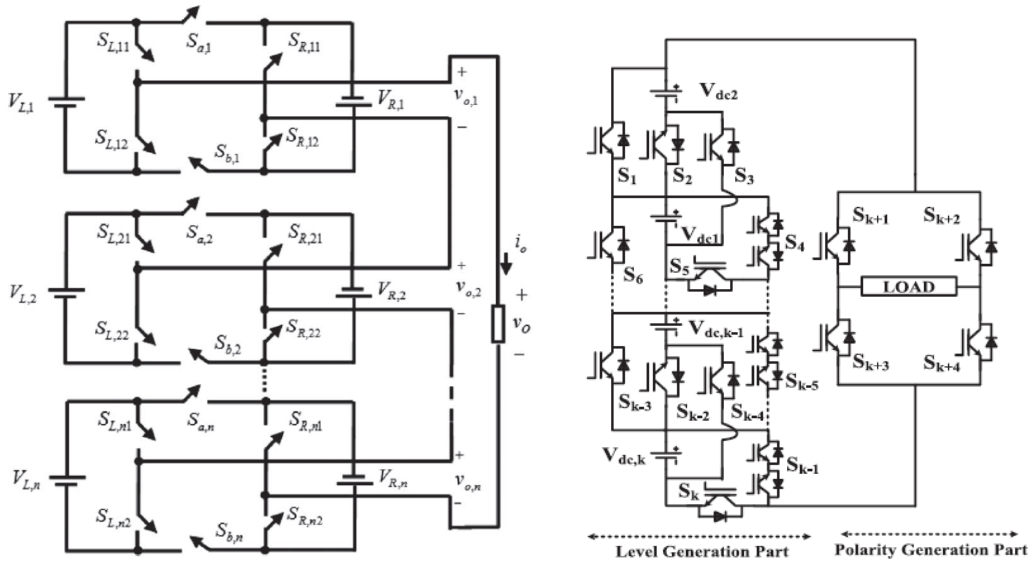
(b)


Capacitor
clamped leg
S6
S5
S4
S3
S2
S1
C2
C1
Vdc
ibus
Vbus
SPFB inverter
Sa
Da
Sb
Db
a
ia
n
van
Sc
Dc
Sd
Dd

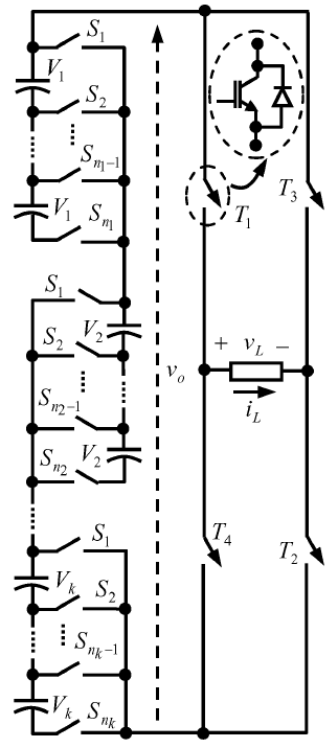
(c)


V0/2
C
V0/2
S5
S7
A
B
S6
S8
L
vbus1
vbus2
vbus
C
Load
vout
Sb1
V1
Sb2
V2
Sa1
Sc1
S1
S3
V3
Sa2
Sc2
Sbn-1
Vn-1
Vn
San-1
Scn-1
S2
S4

(d)



(e) (f)



(g)

Figure 3.1 The MLDCL inverter configurations are based on the integration of (a) a cascaded half-bridge cells, (b) a diode-clamped leg, and (c) a capacitor-clamped leg with a single-phase full-bridge MLI [3], (d) switched series/parallel sources MLI [11], (e) hexagonal switched cell MLI [21], (f) the trinary sequence-based MLI [33], (g) cascaded bipolar switch MLI [7]

3.2.5.2 Symmetrical Reduced Switch Count Topologies With H-bridge

Symmetrical RSC-MLI topologies incorporating H-bridge structures offer an alternative solution by reducing overall hardware complexity while maintaining acceptable output voltage quality. In these topologies, all DC sources have equal magnitudes, and output levels are typically achieved through optimized switching units integrated with H-bridge configurations. The symmetrical structure can contribute to balanced operation and ease of control, while also offering potential advantages in terms of manufacturing, maintenance, and modular integration. The resulting simplified architecture offers promising characteristics in terms of design clarity and practical implementation.

In the following sections, the relevant studies on these topologies are comprehensively analyzed in terms of their design motivations, structural configurations, operating principles, modulation and control strategies, application areas, advantages and limitations, and contributions to literature.

Ceglia et al. (2006) introduce a simplified MLI topology, commonly referred to as the T-Type inverter, to address the inherent complexity of conventional multilevel converters, which require excessive power switches, capacitors, and intricate control systems. The design aims to minimize component count and modulator circuit complexity while maintaining performance in DC-AC conversion. The proposed five-level inverter employs an asymmetrical H-bridge structure with a bidirectional auxiliary switch, utilizing five controlled switches, eight diodes, and two capacitors. The operating principle enables the generation of five distinct output voltage levels by utilizing various switching combinations. For example, specific configurations of the main and auxiliary switches allow the inverter to produce higher or intermediate voltage levels as required. The capacitor voltage divider ensures automatic voltage balancing without external control. Modulation employs a sigma-delta adaptive strategy implemented via an FPGA, enabling switching frequencies from 10 kHz to 200 kHz, with interlock delays to prevent cross-conduction. The topology targets medium-to-high power applications, including uninterruptible power supplies and industrial drives, where reduced hardware complexity is critical. Key advantages include a 37.5% reduction in main switches compared to NPC topologies, 60% fewer diodes, and experimental validation showing 92.4% efficiency with clean output waveforms. Limitations

include reliance on precise FPGA-based control and scalability constraints beyond five levels without structural modifications. The authors highlight superiority over NPC (8 switches, 20 diodes) and capacitor-clamped (10 capacitors) configurations, emphasizing component reduction. The modular extension to n-level configurations using multiple bidirectional switches is theorized but not experimentally verified. This work contributes a hardware-efficient RSC-MLI solution, validated through SPICE simulations and a prototype, demonstrating reduced THD and operational flexibility across frequency ranges, advancing cost-competitive multilevel converters for industrial applications [4].

Choi and Kang (2008) propose a transformerless H-bridge-based MLI topology to address the challenge of achieving low THD in RSC-MLIs without relying on bulky output filters. The design aims to enhance output voltage waveform quality by integrating PWM into the switching strategy of a prior seven-level H-bridge inverter, thereby reducing harmonic distortion. The topology employs seven switches and three symmetrical DC voltage sources, structured around a full-bridge configuration with additional switches to synthesize multiple voltage levels. Multilevel output is achieved through a modified switching sequence in which selected switches operate under PWM control to interpolate voltage steps, thereby generating a quasi-sinusoidal waveform. A carrier-based PWM method at 1 kHz switching frequency is utilized, with switching angles modulated to control harmonic amplitudes. The topology targets PV applications, leveraging their compatibility with multiple DC sources. Key advantages include a 50% reduction in switch count compared to conventional CHB inverters and improved THD through stepped-PWM hybridization. However, THD remains above 5%, necessitating a smaller output filter, while increased switching losses arise from higher-frequency PWM operation. The authors directly compare the topology with conventional CHB designs, highlighting its superior switch economy and reduced filter requirements. Simulation and experimental validation demonstrate a 7-level output with enhanced sinusoidal approximation, confirming its contribution to RSC-MLI research as a cost-effective, filter-optimized solution for PV systems [10].

Ebrahimi et al. (2012) propose a cascaded multilevel converter topology to address the challenges of excessive component count and voltage stress in conventional

MLIs such as NPC, FC, and CHB topologies. The design aims to minimize the number of power electronic components-including switches, IGBTs, diodes, and gate drivers-while maximizing output voltage levels through multilevel module topology. The topology is classified as asymmetrical due to unequal DC source magnitudes, with each multilevel module containing N_{bis} bidirectional switches and DC sources, cascaded to generate positive voltage steps, while full-bridge converters enable bipolar output. Voltage synthesis relies on activating a single bidirectional switch per multilevel module and alternating full-bridge switches to avoid short circuits. A fundamental frequency switching strategy is employed to approximate the reference voltage, though harmonic optimization is not explicitly addressed. The converter targets applications requiring high power quality or utilizing distributed DC sources, such as renewable energy systems with PV panels or fuel cells. Key advantages include reduced component count (24 IGBTs for 125 levels), modular scalability, and lower conduction/switching losses compared to prior topologies. However, it requires multiple isolated DC sources and exhibits increased switch blocking voltages at higher levels. Experimental validation of a 125-level prototype demonstrates a peak output of 400 V with 5.9% THD, confirming its efficacy in balancing component reduction with performance. This work advances RSC-MLI research by introducing a modular, asymmetrical architecture optimized for hardware efficiency, validated through both analytical loss models and experimental results [14].

Najafi and Yatim (2012) introduce a reversing voltage MLI topology to address the challenges of excessive component count, control complexity, and voltage balancing in conventional MLIs such as NPC, FC, and cascade topologies. The design aims to minimize semiconductor switches, gate drives, and isolated DC sources while enhancing reliability by segregating high-frequency switching (level generation) and low-frequency polarity reversal (H-bridge-based polarity generation). Classified as a symmetrical topology with equal DC voltage sources, the Reversing Voltage structure combines a high-frequency stage generating unipolar voltage levels and a full-bridge converter operating at line frequency to produce bipolar output. Voltage synthesis involves activating specific high-frequency switches (e.g., 10 switches for seven levels) to generate positive steps, while the H-bridge alternates the polarity without high-frequency switching,

achieving N*N* levels through modular expansion of the level generation stage. Phase-disposition SPWM is employed, requiring only half the carrier signals (three for seven levels) compared to conventional methods, simplifying control implementation. The topology targets high-voltage applications such as FACTS, HVDC, PV systems, and uninterruptible power supplies. Key advantages include reduced component count (e.g., 10 switches and 3 DC sources for seven levels), modular scalability, lower conduction losses (4-5 conducting switches per level vs. 6 in cascade topologies), and compliance with IEEE 519 harmonic standards (3.85% THD for R loads). Limitations include dependency on isolated DC sources and absence of voltage-balancing mechanisms. Direct comparisons with NPC, FC, and cascade inverters demonstrate fewer switches and reduced components (e.g., 84 switches for 48-pulse STATCOM vs. 48 switches with transformers). Experimental validation of a seven-level prototype, operating with a peak-to-peak voltage of 300 V and a switching frequency of 4 kHz, confirms its effective performance with filtered output THD below 4%. This work advances RSC-MLI research by integrating modularity with hybrid switching strategies, offering a cost-effective solution for high-power applications, validated through component reduction metrics and experimental harmonic performance [15].

Nilkar, Babaei, and Sabahi (2012) address the perennial challenge of component minimization in MLIs by introducing a cascaded topology employing four-level basic cells to reduce switch count while enhancing voltage resolution. The design specifically targets hardware simplification through modular expansion, achieving 21 output levels with only 12 IGBTs in a two-cell asymmetric configuration-a 40% reduction compared to conventional CHB designs. Classified as an asymmetrical H-bridge-based topology, the structure comprises series-connected four-level cells (each containing two DC sources and four switches) and an H-bridge for bipolar voltage generation. Voltage synthesis occurs through sequential activation of switches in each cell, enabling four discrete states per module: direct source connection, series combination, bypass, and zero-voltage modes. Fundamental frequency staircase modulation minimizes switching losses by operating devices at 50 Hz, with H-bridge switches reversing polarity once per cycle. The topology targets renewable energy integration, including PV systems and fuel-cell converters, where modularity and low conduction losses (attributed to single-switch

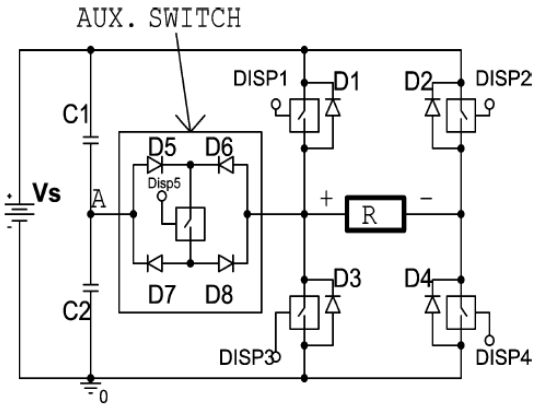
conduction per cell state) are critical. Advantages include scalability to 31 levels via binary-scale DC sources and 21-level generation with unary sources, though asymmetric operation necessitates heterogeneous DC sources, complicating practical implementation. Comparative analysis against CHB inverters reveals superior switch efficiency: for 16 output steps, the proposed topology requires 12 switches versus 20 in CHB, with fewer source magnitude variations in binary mode. Experimental validation through PSCAD simulations demonstrates a 21-level output voltage with 1.0% THD under resistive-inductive (RL) load, consisting of 107 Ω resistance and 55mH inductance, confirming the topology's effectiveness in achieving a balance between waveform quality and component efficiency. This work advances RSC-MLI research by demonstrating scalable voltage resolution with minimized switching hardware, validated through modular cell cascading and low-frequency control strategies [16].

Kangarlu and Babaei (2013) propose a generalized cascaded MLI topology, referred to as the Two Switched Enable Generation inverter, to address the trade-off between the quality of the output voltage waveform and the number of required devices in high-power applications. The design aims to minimize switching components by cascading modular submultilevel inverters, each comprising N_{dc} DC sources and N_{dc} + 2 switches, followed by an H-bridge for polarity reversal. Classified as a symmetrical or asymmetrical H-bridge-based topology, it synthesizes voltage levels through sequential activation of bidirectional and unidirectional switches in submodules. In symmetrical mode, equal DC sources generate uniform voltage steps, while asymmetrical configurations employ geometrically scaled sources to maximize levels. A staircase modulation strategy operates switches at fundamental frequency, aligning output with reference voltage while minimizing transitions. Targeted for industrial drives (e.g., pumps, compressors) and renewable energy integration, the topology reduces IGBT counts by 25-50% compared to CHB designs, with 12 IGBTs required for a 31-level asymmetric prototype versus 16 in prior works. Advantages include modular scalability, lower conduction losses (12 W vs. 15.5 W in CHB), and reduced gate drivers; however, voltage stress on H-bridge switches limits high-voltage applicability without series-connected devices. Experimental validation demonstrates 1.44% voltage THD and 0.2% current THD under RL load. This work

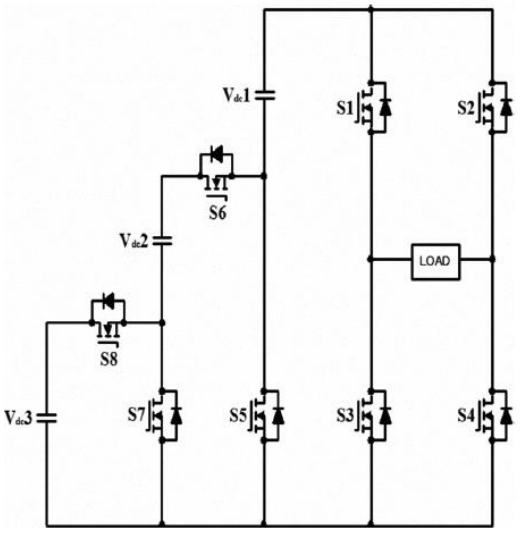
advances RSC-MLI literature by optimizing component efficiency while maintaining waveform fidelity, validated through PSCAD simulations and a 150 V, 31-level hardware prototype [17].

Toupchi Khosroshahi (2014) proposes a MLI topology, known as Crisscrossed Cascade, to address the high component count and complexity of conventional CHB converters, particularly critical for medium-voltage applications requiring modularity and harmonic suppression. The design aims to reduce switch count, peak inverse voltage, and conduction losses while enhancing waveform quality. The topology employs an asymmetrical H-bridge structure with bidirectional switches, utilizing 2 x N_{dc} + 4 switches and 3 x N_{dc} + 4 IGBTs for N_{dc} DC sources in symmetric mode, while asymmetric configurations with binary scaling achieve higher levels (e.g., 31 levels with 4 DC sources). Voltage synthesis occurs through modular basic units, each combining two DC sources via four switches, with the H-bridge inverting polarity. A vertical phase-shifted SPWM, implemented via a dsPIC30F4011 microcontroller and HCPL316 gate drivers, controls switching states. The inverter targets renewable energy systems, microgrids, and industrial drives, offering advantages such as a 37.5% switch reduction versus CHB, lower peak inverse, and modular scalability. Experimental results demonstrate 13-level symmetric (10.7% THD) and 31-level asymmetric (5.81% THD) outputs with reduced conduction losses. Limitations include dependency on multiple DC sources and complex asymmetric scaling. The work contributes a validated RSC-MLI solution, experimentally achieving 92.0V output under RL load, advancing hardware efficiency and harmonic performance for medium-voltage applications [20].

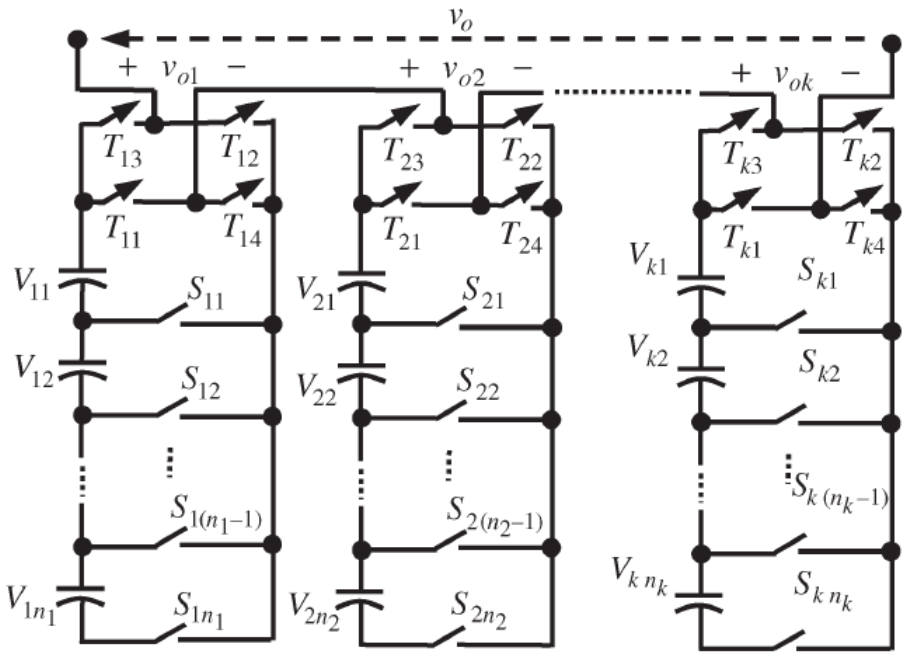
The "Symmetrical Reduced Switch Count Topologies With H-bridge" discussed above are illustrated in Figure 3.15.


AUX. SWITCH
DISP1
D1
D2
DISP2
C1
D5
D6
Disp5
Vs
A
R
D7
D8
C2
D3
D4
DISP3
DISP4
0

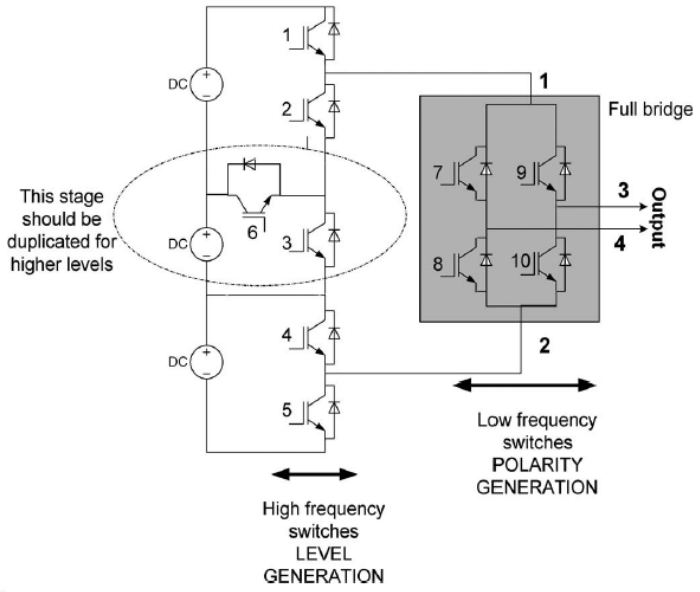
(a)


S1
S2
S6
LOAD
S8
S7
S5
S3
S4

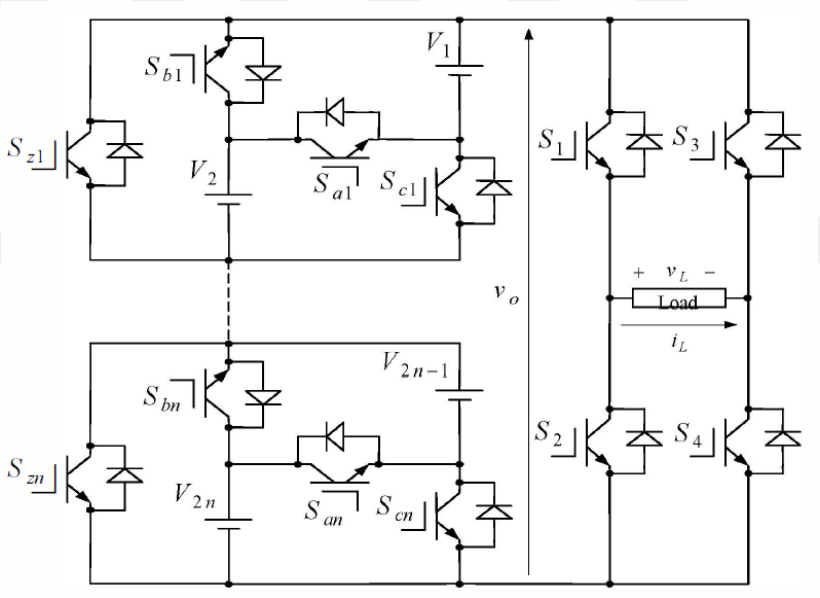
(b)


v_o
v_{o1}
v_{o2}
v_{ok}
T_{13}
T_{12}
T_{11}
T_{14}
T_{23}
T_{22}
T_{21}
T_{24}
T_{k3}
T_{k2}
T_{k1}
T_{k4}
V_{11}
S_{11}
V_{12}
S_{12}
$S_{1(n_1-1)}$
V_{1n_1}
S_{1n_1}
V_{21}
S_{21}
V_{22}
S_{22}
$S_{2(n_2-1)}$
V_{2n_2}
S_{2n_2}
V_{k1}
S_{k1}
V_{k2}
S_{k2}
$S_{k(n_k-1)}$
V_{kn_k}
S_{kn_k}

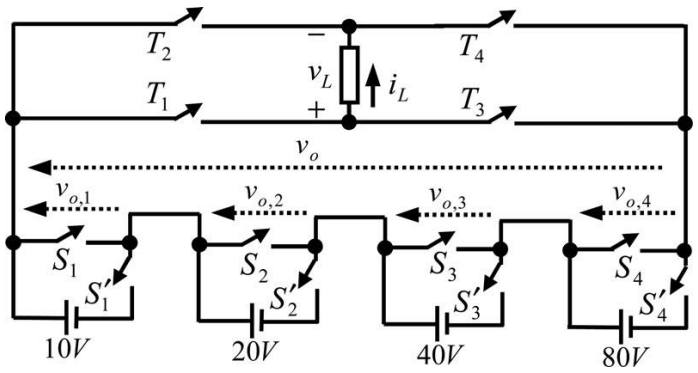
(c)


DC
1
2
6
3
4
5
7
9
8
10
Full bridge
Output
This stage should be duplicated for higher levels
Low frequency switches POLARITY GENERATION
High frequency switches LEVEL GENERATION

(d)


S_{b1}
V_1
S_{z1}
V_2
S_{a1}
S_{c1}
S_1
S_3
v_o
v_L
Load
i_L
V_{2n-1}
S_{bn}
S_{zn}
V_{2n}
S_{an}
S_{cn}
S_2
S_4

(e)


T_2
T_4
T_1
T_3
v_L
i_L
v_o
$v_{o,1}$
$v_{o,2}$
$v_{o,3}$
$v_{o,4}$
S_1
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S_4'
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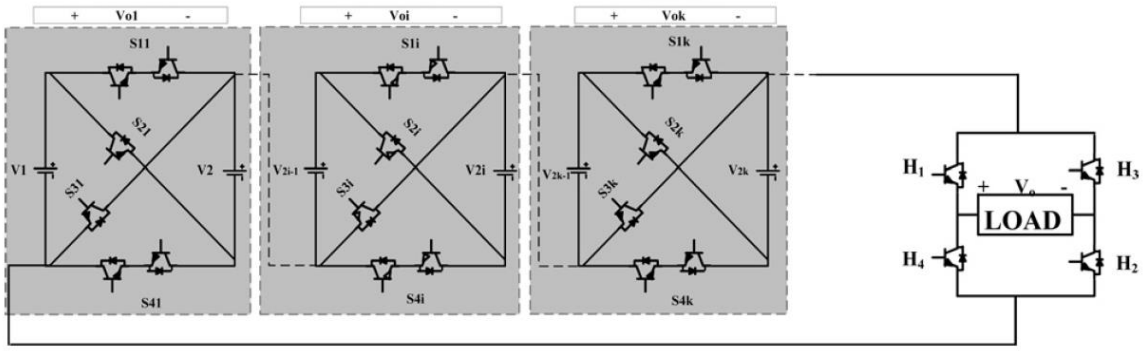
20V
40V
80V

(f)



(g)

Figure 3.2 (a) T-type MLI [4], (b) H-bridge cell based MLI [10], (c) multilevel module MLI [14], (d) reversing voltage MLI [15], (e) Nilkar MLI [16], (f) two switched enable generation MLI [17], (g) crisscross cascade MLI [20]

3.2.5.3 Asymmetrical Reduced Switch Count Topologies Without H-bridge

Asymmetrical RSC-MLI topologies without H-bridge structures represent a distinctive design approach that aims to generate high output voltage levels using a minimal number of switching devices. By eliminating the need for additional H-bridge stages, these topologies enable the development of more compact and cost-effective inverter systems. Furthermore, by utilizing asymmetrical DC voltage ratios, they can achieve an increased number of output levels, which in turn reduces harmonic content and eases filtering requirements.

In the following sections, the relevant studies on these topologies are comprehensively analyzed in terms of their design motivations, structural configurations, operating principles, modulation and control strategies, application areas, advantages and limitations, and contributions to literature.

Babaei (2008) addresses the challenge of excessive switch counts in multilevel converters by proposing a cascaded sub multilevel topology, known as the Cascaded Bipolar Switch inverter. The design aims to minimize switches, capacitors, and standing voltage while generating high step counts. A 53-level prototype employs 22 IGBTs and 6 DC sources in an asymmetrical configuration with an H-bridge for polarity reversal. Voltage synthesis is achieved through bidirectional switches in series-connected submodules, controlled via staircase modulation implemented via a microcontroller. Experimental results demonstrate a voltage THD of 3.17% and current THD of 0.23%. Limitations include bidirectional switch complexity and medium-voltage scalability constraints due to

H-bridge requirements. The study contributes a modular, component-optimized solution validated through a 53-level prototype, advancing RSC-MLI efficiency in high-step applications [7].

The Packed U Cells multilevel converter topology proposed by Ouneijar et al. (2011) addresses the challenge of excessive component counts in conventional multilevel topologies, such as NPC and FC converters, by optimizing hardware efficiency. The design motivation centers on reducing active and passive components-utilizing six switches and two capacitors for a seven-level configuration-while maintaining high power quality. Classified as asymmetrical topology without an H-bridge, the Packed U Cells employs unequal capacitor voltages to synthesize seven output levels via eight switching states, including redundant zero-voltage states for device stress reduction. A seven-level SPWM scheme operating at a switching frequency of 1 kHz, combined with a lookup-table-based control strategy, regulates the auxiliary capacitor voltage to maintain voltage balancing. Intended for applications such as motor drives and grid-connected systems, the topology offers advantages including a critical reduction in switches and capacitors compared to FC and NPC topologies, compact design, and modular scalability-31 levels with ten switches and four capacitors. Limitations include reliance on precise capacitor voltage regulation, though experimental results confirm stable operation under load transients. Direct comparisons highlight Packed U Cells' superiority: it requires 50% fewer switches and 67% fewer capacitors for the seven-level output than FC converters. Simulation and experimental validation demonstrate a 24.32% THD in load voltage, validating its efficacy. This work contributes a cost-effective, scalable multilevel solution that advances RSC-MLI research by demonstrating hardware minimization without compromising output quality, supported by rigorous simulation and dSpace DS1103-based experimental verification [12].

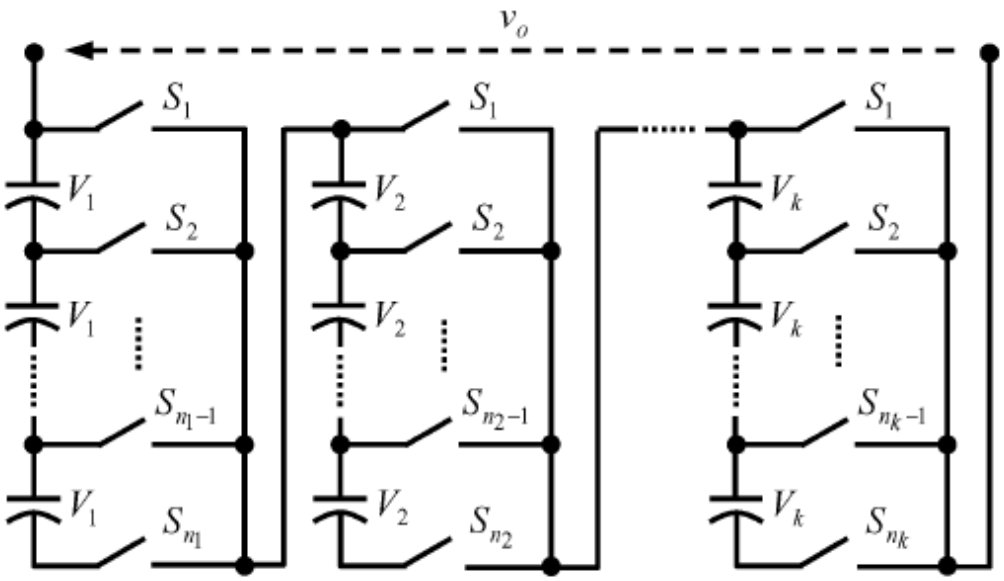
Samadaei et al. (2016) advance asymmetric MLI research by introducing an Envelope Type module to mitigate component count and voltage stress challenges in high-power applications. The topology aims to eliminate H-bridge dependency for polarity reversal while reducing semiconductors, achieving 13 output levels per module with four asymmetric DC sources and 10 switches. Classified as an asymmetrical H-bridge-free topology, the Envelope Type synthesizes ±6V through

bidirectional switches that reconfigure DC source connections via distinct switching paths, avoiding short circuits through diode-blocking mechanisms. SHE PWM with six switching angles per quarter-wave eliminates 3rd-19th harmonics, operating at 50 Hz fundamental frequency with optimized angles to achieve 3.46% simulated THD. Targeted for HVDC and renewable energy systems, the design reduces components by 16.7% versus conventional MLIs, requiring only 5 x (N_{level} - 1) / 6 switches and (N_{level} - 1) / 3 DC sources for N_{level} levels. Advantages include inherent bipolar operation, modular scalability (25 levels with two cascaded modules), and 96.56% efficiency under 150Ω load; however, asymmetric DC source requirements complicate practical deployment. Comparative analysis shows superiority over NPC, CHB, and U-cell topologies, reducing TSV to 10 x (N_{level} - 1) / 6 V versus 2 x (N_{level} - 1) V in CHB. Experimental validation with ATMEGA16-controlled IGBTs confirms 4.54% THD under RL loads, adhering to IEEE 519 standards without filters. This work contributes a modular RSC-MLI architecture that balances harmonic performance and hardware economy, validated through 650V/13-level hardware prototypes and MATLAB simulations [31].

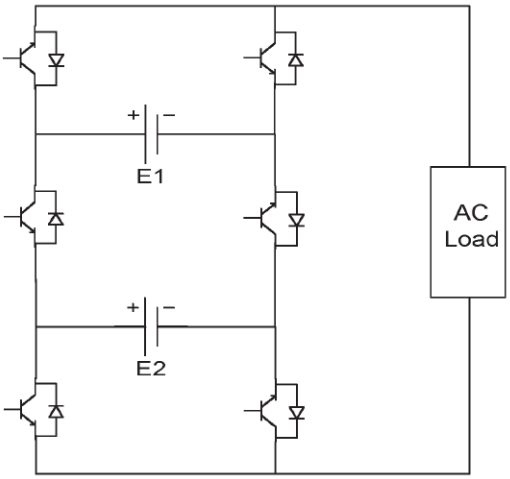
The Square T-Type module proposed by Samadaei et al. (2017) addresses the persistent challenge in RSC-MLI research of achieving high-level output synthesis with minimized switch count and reduced circuit complexity. The primary design motivation centers on developing a MLI topology that eliminates the need for a traditional H-bridge while still generating both positive and negative voltage levels, thereby improving hardware efficiency. Structurally, the topology is an asymmetrical configuration without an H-bridge, composed of 12 switches and four unequal DC sources organized to produce 17 distinct voltage levels. Its operating principle relies on a novel circuit arrangement where two back-to-back T-type cells, connected in a square formation, synthesize the output voltage through a controlled switching sequence that inherently supports both polarities without additional polarity generation circuits. The modulation and control strategy employs the NLC method, which enhances output waveform quality with reduced computational complexity. The topology is specifically targeted at renewable energy applications, notably large-scale PV systems, where high power density and reduced component count are critical. The proposed module offers notable advantages, including a reduced THD, a compact design free of auxiliary polarity-reversing circuits, and

modular scalability for higher voltage levels. A limitation, as indicated, is the complexity introduced by the asymmetrical DC source configuration, which may necessitate precise voltage management. Compared to conventional CHB and T-type topologies, the Square T-Type module demonstrates superior performance by achieving 17 levels with fewer components and simpler structure. The authors' contribution is significant in that they introduce a new modular building block capable of generating multiple voltage levels with inherent polarity inversion, validated through both simulation and experimental results, thereby advancing the field of RSC-MLI design with a practical and scalable solution that addresses both structural and operational inefficiencies prevalent in existing topologies [32].

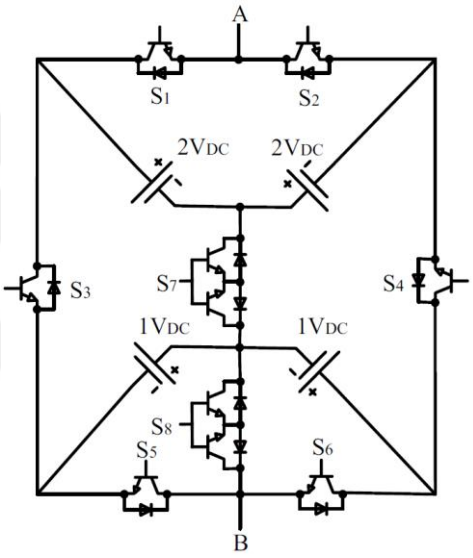
The "Asymmetrical Reduced Switch Count Topologies Without H-bridge" discussed above are illustrated in Figure 3.16.



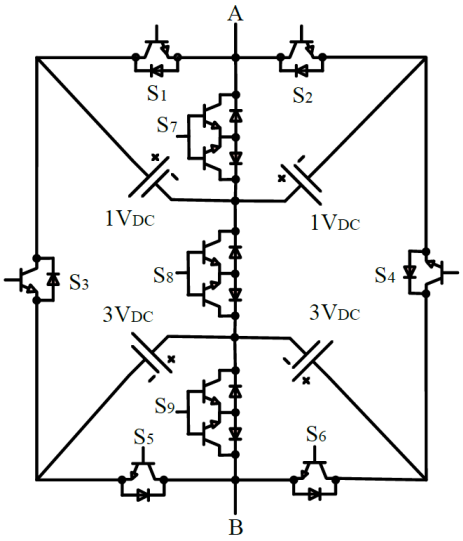
(a)


E1
E2
AC
Load

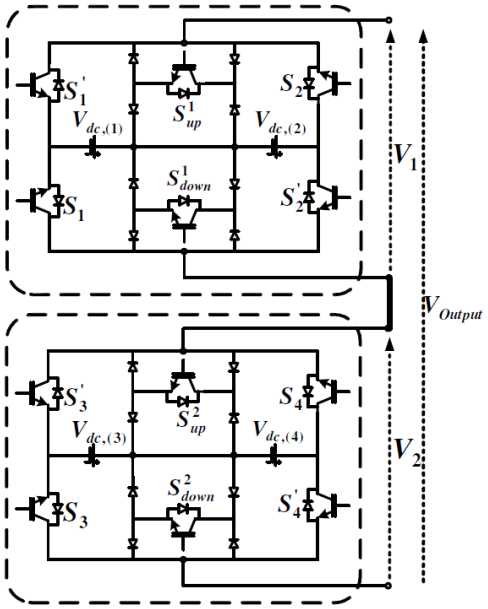
(b)


A
S1
S2
2VDC
2VDC
S3
S7
S4
1VDC
1VDC
S8
S5
S6
B

(c)


A
S1
S2
S7
1VDC
1VDC
S3
S8
S4
3VDC
3VDC
S9
S5
S6
B

(d)



(e)

Figure 3.3 (a) Cascaded bipolar switch MLI [7], (b) packed u cells MLI [12], (c) envelope type MLI [31], (d) square T-type MLI, (e) Mokhberdoran MLI [32]

3.2.5.4 Symmetrical Reduced Switch Count Topologies Without H-bridge

Symmetrical RSC-MLI topologies without H-bridge structures aim to produce high-quality output with fewer switching devices while maintaining a balanced configuration in which all DC sources are of equal magnitude. Voltage level generation is typically achieved through the coordinated operation of serially connected identical cells, resulting in acceptable harmonic performance.

In the following sections, the relevant studies on these topologies are comprehensively analyzed in terms of their design motivations, structural configurations, operating principles, modulation and control strategies, application areas, advantages and limitations, and contributions to literature.

In their 2013 study, Farhadi Kangarlu and Babaei propose a novel structure known as the Cross-Switched MLI to address the challenge of high switch counts in conventional MLI topologies. The design maintains output voltage quality while significantly reducing the number of power switches by utilizing a symmetric structure composed of low-voltage IGBTs and uniquely cross-connected DC sources. Unlike previous reduced-switch configurations that often require high-voltage semiconductors, the proposed topology ensures full voltage synthesis

capability without exceeding low-voltage switch limits, making it inherently suitable for high-voltage applications. The inverter operates under the NLC strategy, a fundamental-frequency modulation technique that minimizes switching events by selecting the voltage level closest to the sinusoidal reference. Experimental implementation of an 11-level, 220 V_{rms} inverter prototype validates the design, achieving 94.4% efficiency, 1240 V TSV, and low THD levels. Furthermore, although only one switching combination per level was used in the tests, the design allows redundant switching combinations that can be selected to minimize switching transitions or balance switch utilization. Compared to classical symmetric CHB inverters and other modern reduced-switch topologies, the Cross-Switched MLI exhibits fewer switches (12 vs. 20 for CHB), fewer devices in the conduction path, and lower TSV, all while avoiding high-voltage stress on switches. With these features, the proposed topology offers a compelling solution for industrial drives, renewable energy conversion, and other high-voltage power processing scenarios. This contribution enriches the RSC-MLI literature by balancing performance, efficiency, and modularity within a compact and scalable framework [88].

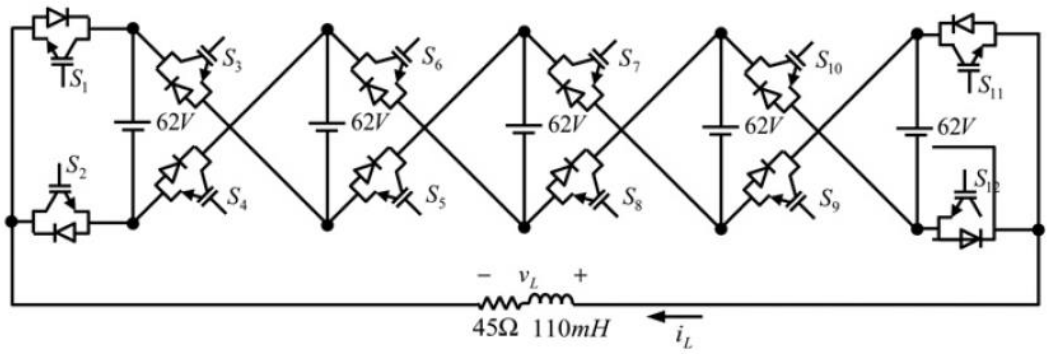
Mokhberdoran and Ajami (2014) address the challenge of excessive component counts and circuit complexity in conventional MLIs by proposing a modular cascaded topology optimized for high voltage levels with minimal switches and DC sources. The design aims to minimize semiconductor components while maximizing output levels through configurable symmetric and asymmetric DC source arrangements. The fundamental block employs six IGBTs and two DC sources, classified as an asymmetrical modular topology without an H-bridge. Voltage synthesis occurs via series-connected blocks, where symmetric operation generates ($4 \times N_{block} + 1$) levels per N_{block} block (e.g., nine levels with two blocks), while asymmetric modes-using three DC source scaling methods (geometric, binary, and septenary)-achieve exponential level growth (e.g., 49 levels with two blocks via (7^{Nblock}) progression). A multicarrier PWM scheme with 1 kHz switching frequency and a dsPIC30F4011-based controller generates gate pulses, enabling selective high-/low-frequency switching across blocks to balance losses. Intended for high-voltage industrial drives, renewable energy systems, and grid applications, the topology offers a 25-50% reduction in IGBT count versus CHB. Limitations

include dependency on isolated DC sources and higher peak inverse voltage in asymmetric modes. Comparative analysis highlights a 31-level configuration requiring 12 IGBTs (vs. 16 in CHB) with 20-30% lower conduction losses and normalized peak inverse voltage of 3/16 (third method) versus 5/16 for CHB. Experimental validation demonstrates 9-, 25-, 31-, and 49-level outputs with a two-block prototype, confirming THD reduction and modular scalability. This work advances RSC-MLI research by demonstrating a scalable, loss-optimized architecture validated through simulation and hardware, achieving high-level output with 50% fewer switches than conventional topologies [23].

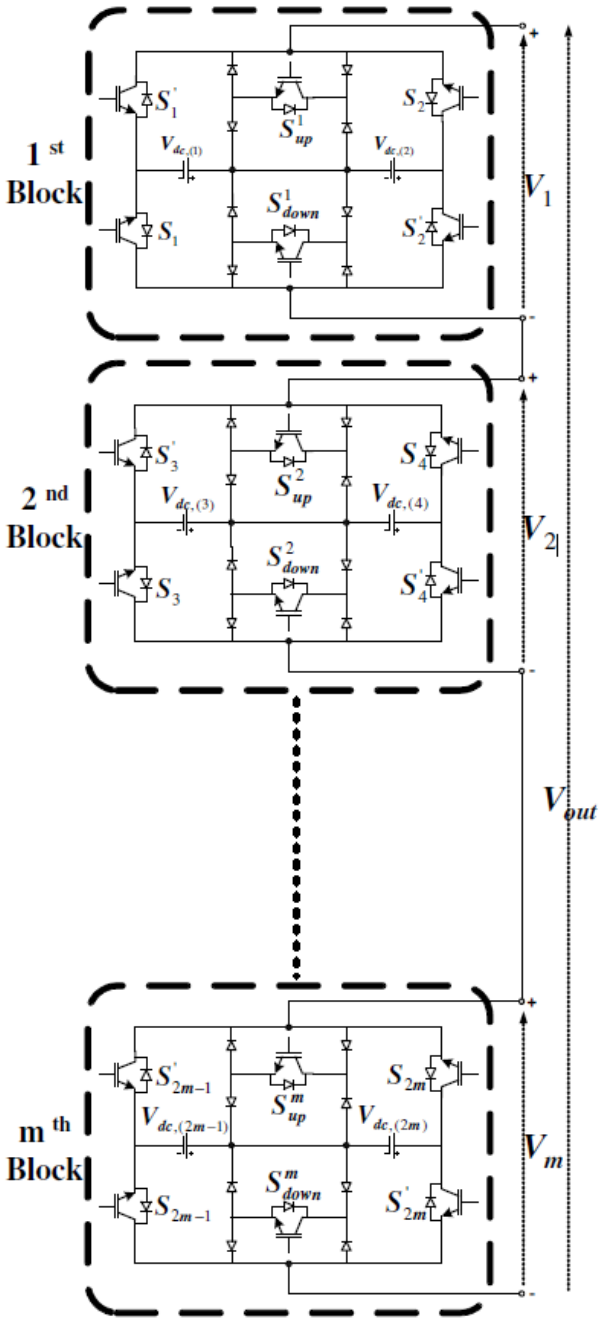
Babaei et al. (2014) propose a novel cascaded MLI topology to address the challenges of component count reduction and cost optimization in medium-voltage high-power applications. he proposed design seeks to reduce the quantity of IGBTs, gate driver circuits, and DC voltage sources, while simultaneously lowering the voltage stress imposed on the switching devices. General topology employs (2 x N_{dc}) asymmetrical DC voltage sources and (4 x N_{dc} + 2) unidirectional switches, structured as developed H-bridge modules with cascaded asymmetrical DC sources. The system forms output voltage by arranging DC sources in additive or subtractive combinations using unidirectional switches, while preventing the concurrent conduction of complementary switches to eliminate short-circuit risks. A fundamental frequency switching control strategy is implemented, where a sinusoidal reference is compared with available voltage levels to select the nearest output state, reducing switching losses. Designed for medium-voltage applications, the topology was validated using a 31-level prototype delivering up to 225 V, utilizing four DC sources and ten switches. Key advantages include reduced IGBT count (e.g., 14 switches for 127 levels) and lower blocking voltage compared to conventional topologies. However, the design necessitates a higher variety of DC source magnitudes, increasing sourcing complexity. The modular structure allows scalability, demonstrated through 7-, 31-, and 127-level configurations. Experimental results confirm 31-level operation with 0.94% voltage THD, 0.19% current THD, and 92.4% efficiency under RL load. This work advances RSC-MLI research by providing a scalable asymmetrical H-bridge architecture with verified performance metrics, balancing component reduction with practical voltage synthesis capabilities [24].

Gupta and Jain (2014) propose a cascaded MLI topology, known as Switched DC Sources, to address the escalating component count in conventional MLIs for high-power applications, emphasizing switch reduction without compromising waveform quality. The design targets minimization of power switches and gate drivers while maintaining symmetric source utilization. The generalized topology utilizes 2 x N_{dc} + 2 power switches—resulting in, for instance, six switches for a five-level configuration—and N_{dc} isolated and symmetrical DC sources. Unlike H-bridge-based structures, the design alternates the polarity of the sources using complementary switching pairs, thereby eliminating the need for H-bridge cells. Voltage synthesis leverages eight switching modes to generate $\pm V_{dc}$, $\pm 2V_{dc}$, and zero levels, achieved by additive combinations of DC sources via unidirectional-blocking switches. A multicarrier PWM scheme with alternate phase opposition disposition is implemented, where high-voltage switches operate at fundamental frequency (50 Hz) and low-voltage switches at 1 kHz, balancing conduction and switching losses. The topology suits renewable energy interfaces, medium-voltage drives, and EVs requiring isolated DC sources. Key advantages include a significant reduction in switches compared to CHB topologies and lower switching losses (half of CHB). However, limitations include dependency on isolated sources, reduced fault tolerance, and variable switch costs due to higher voltage ratings. Comparative analysis highlights modular scalability and a 36.89% simulated voltage THD for a five-level prototype, validated experimentally with 24 V sources and RL load. This work advances RSC-MLI research by demonstrating a switch-efficient, asymmetrical topology with validated loss distribution and operational feasibility, though trade-offs in source isolation and fault tolerance persist [25].

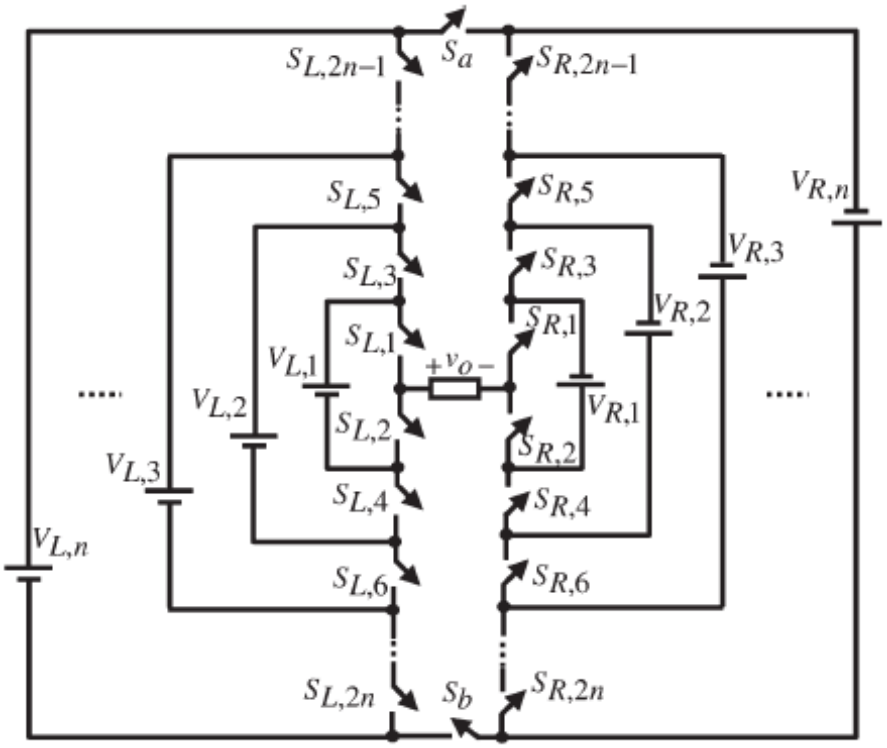
The "Symmetrical Reduced Switch Count Topologies Without H-bridge" discussed above are illustrated in Figure 3.17.


S_1
S_3
S_6
S_7
S_{10}
S_{11}
62V
62V
62V
62V
62V
S_2
S_4
S_5
S_8
S_9
S_{12}
v_L
45Ω 110mH
i_L

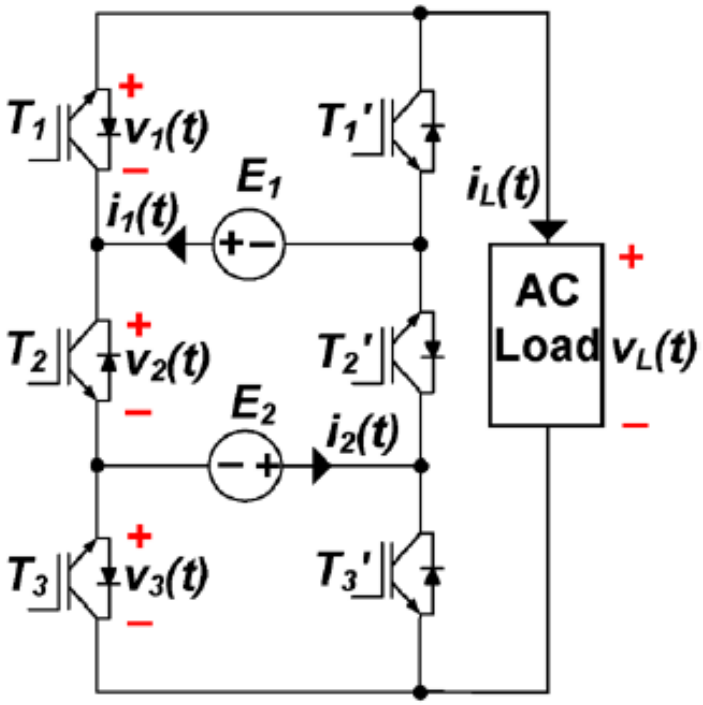
(a)


1 st Block
2 nd Block
m th Block
S'_1
S'^1_{up}
S_2
$V_{dc,(1)}$
$V_{dc,(2)}$
S^1_{down}
S_1
S'_2
S'_3
S'^2_{up}
S_4
$V_{dc,(3)}$
$V_{dc,(4)}$
S^2_{down}
S_3
S'_4
S'_{2m-1}
S'^m_{up}
S_{2m}
$V_{dc,(2m-1)}$
$V_{dc,(2m)}$
S^m_{down}
S_{2m-1}
S'_{2m}
V_1
V_2
V_m
V_{out}

(b)



(c)



(d)

Figure 3.4 (a) Cross switched sources MLI [88], (b) Mokhberdoran MLI [23], (c) Babaei MLI [24], (d) switched DC sources MLI [25]

3.3 Modulation Strategies for Multilevel Inverters and THD Minimization Techniques

Modulation strategies play a critical role in determining the performance, harmonic profile, and dynamic response of MLIs. Depending on the switching frequency and control objectives, a variety of modulation techniques have been developed to optimize switching losses, THD, and voltage waveform quality.

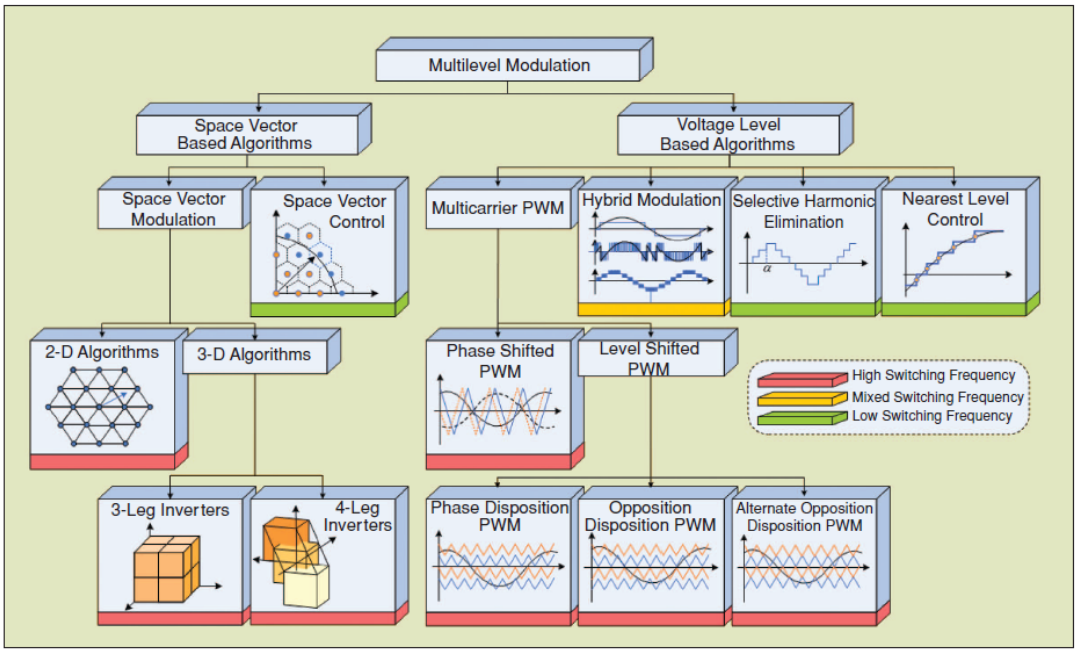


Figure 3.1 Classification of modulation techniques for MLIs [60]

Figure 3.18 presents a systematic classification of widely adopted modulation techniques for MLIs. These methods are categorized into two main groups based on their operational principles: Space Vector-Based Algorithms and Voltage Level-Based Algorithms.

Space vector-based algorithms operate within the state-space domain, focusing on the synthesis of voltage vectors. Two major methods within this group are SVM and Space Vector Control. These can be further subdivided into 2D and 3D algorithms, typically applied to 3-leg and 4-leg inverter topologies, respectively.

Voltage level-based algorithms operate in the time domain and generate output waveforms by controlling discrete voltage levels. Key techniques in this category include:

- Multicarrier PWM methods, which are divided into Phase-Shifted and Level-Shifted PWM. The latter includes variants such as Phase Disposition, Phase Opposition Disposition, and Alternate Phase Opposition Disposition.
- SHE, which selectively targets specific harmonic components for elimination.
- NLC, where the switching state closest to the reference waveform is selected at each instant.
- Hybrid Modulation Techniques, which combine features from different strategies to enhance performance, flexibility, or efficiency.

Furthermore, the methods are also labeled based on their switching frequency characteristics:

- Low switching frequency techniques are preferred for high-power applications due to reduced switching losses.
- High switching frequency approaches provide improved output waveform quality and dynamic response.
- Mixed-frequency strategies strike a balance between efficiency and harmonic performance, enabling versatility across a range of applications [60].

3.3.1 Fundamental Switching Frequency Modulation

In this section, three major control techniques categorized under Fundamental Switching Frequency Modulation-namely SHE, NLC, and Nearest Vector Control (NVC)-will be comprehensively analyzed. Such techniques are particularly critical in MLIs for achieving reduced harmonic distortion and producing high-quality output waveforms. The subsequent subsections will examine each method in detail, addressing their theoretical foundations, operational principles, and practical implementations.

3.3.1.1 Selective Harmonic Elimination

In 1973, H. S. Patel and R. G. Hoft introduced a comprehensive theoretical framework for harmonic elimination and voltage regulation in power electronic systems, as outlined in references [89], [90]. And their methodology established

generalized principles for optimizing waveform quality and maintaining voltage stability, laying the groundwork for advanced modulation strategies in MLIs and related applications.

SHE is a fundamental switching-frequency-based modulation strategy designed to eliminate specific low-order harmonics from the output voltage waveform of power electronic converters. The SHE method aims to maintain the desired amplitude of the fundamental component while suppressing selected harmonics via precomputed switching angles obtained from the Fourier decomposition of the waveform.

In its most common formulation, SHE assumes quarter-wave symmetry, leading to a simplified set of cosine-only equations for odd harmonics. This set of nonlinear transcendental equations is typically solved using numerical or optimization methods.

Initially proposed for two-level inverters, SHE has been successfully extended to multilevel topologies such as CHB inverters, which offer enhanced output voltage quality and superior harmonic control. In these systems, waveform formulations vary based on symmetry and voltage level structure, significantly affecting the complexity of the harmonic elimination problem. Quarter-wave symmetry allows for simplified equations by considering only odd cosine harmonics, while half-wave symmetry includes both sine and cosine terms, enabling greater harmonic flexibility. Non-symmetrical waveforms, though offering full harmonic control, result in highly complex solutions due to the inclusion of all harmonic components. This complexity further increases in systems with unequal or variable voltage levels, where either fixed but scaled sources or dynamically changing DC voltages are introduced as additional variables in the solution space, requiring advanced optimization techniques and increased computational effort [91].

Although SHE was initially applied to two-level inverters, it has been successfully extended to multilevel series-connected voltage-source inverters. Li et al. [92] proposed two principal techniques to address the nonlinear transcendental equation system encountered in multilevel SHE applications. The first is the phase-shift harmonic suppression method, which is employed to provide effective initial estimates for the Newton-Raphson iteration algorithm. This approach significantly enhances the convergence behavior, especially in systems with many switching

angles. The second technique is known as the mirror surplus harmonic method. In this method, harmonic components generated by one cell are effectively canceled by introducing counter-phase harmonics from another cell. This cancellation mechanism proves particularly effective in two-cell configurations, where it enables the elimination of low-order harmonics with reduced computational complexity.

The number of controllable harmonics is directly linked to the total number of switching angles. For instance, two cells with five angles each in a quarter cycle allow up to ten harmonics to be targeted [92].

These techniques enable SHE to achieve high harmonic performance in both single-phase and three-phase systems, even at low switching frequencies - making SHE a compelling option for medium- and high-power industrial applications.

One major limitation of the classic SHE technique is its focus on eliminating only a few selected harmonics while leaving others uncontrolled. This is particularly problematic in high-power applications where grid codes specify strict amplitude limits for a broader range of harmonics. To overcome this, a flexible SHE-derived technique known as Selective Harmonic Mitigation (SHM) has been proposed [93].

Instead of forcing certain harmonics to zero, SHM aims to keep all harmonics below predefined limits and restricts the THD. The problem is reformulated as an optimization task, often solved using general-purpose heuristic algorithms such as simulated annealing. This approach is highly suitable for complying with standards that impose limits up to the 50th harmonic. SHM thus enables high-quality grid integration without the need for bulky line filters, offering a practical and flexible modulation alternative, especially for three-level inverters [93].

In conclusion, the SHE technique is a highly effective modulation strategy for high-power converter systems, offering selective suppression of low-order harmonics while maintaining the fundamental frequency component. Its application to MLI topologies significantly enhances output voltage quality and reduces both switching losses and filtering requirements. However, the practical deployment of SHE is constrained by the complexity of the solution space, the sensitivity to initial conditions, and challenges in maintaining continuous solution trajectories. Therefore, more flexible and regulation-oriented variants like SHM extend the

theoretical advantages of SHE into broader and more demanding application domains [91], [92], [93].

3.3.1.2 Nearest Level Control

NLC is a widely adopted modulation strategy in MLIs, known for its low switching frequency and structural simplicity. The fundamental principle of NLC lies in selecting the closest discrete voltage level to the instantaneous reference voltage, thereby eliminating the need for complex PWM schemes [94].

In this technique, the reference voltage is sampled at each control interval, and a rounding function is used to determine the closest achievable output level. This process is independently applied to each phase, enabling a staircase-like output waveform that approximates the reference sinusoid with minimal computational burden [94]. NLC is especially effective in reducing switching losses and achieving high-quality voltage output with low transition rates [95].

However, traditional NLC methods may present limitations such as increased harmonic distortion, voltage ripple, and unsuppressed internal currents when implemented in converters with a lower number of levels. To address these issues, advanced variants of NLC have been developed. These include calculating the number of active levels in the upper and lower arms based on both the reference output voltage and internal feedback signals, thus enhancing the modulation fidelity [95].

Furthermore, in converters with many output levels, the use of NLC allows for direct synthesis of voltage steps without modulation layers. This significantly reduces control complexity while ensuring precise torque control and waveform generation with minimal ripple, especially in high-performance drive systems [96].

3.3.1.3 Nearest Vector Control

NVC is a fundamental switching frequency control strategy applied to MLIs, where the reference voltage vector in the α-β plane is approximated by directly selecting the nearest available discrete voltage vector from the converter's state-space. Unlike conventional modulation techniques that rely on time-averaged switching sequences, NVC eliminates the need for temporal decomposition of the reference and is thus categorized as a control method rather than a modulation scheme [2], [97].

The core idea behind NVC is to exploit the extensive set of voltage vectors inherent to multilevel converters. The α-β plane is partitioned into regions (e.g., hexagonal Voronoi cells), each corresponding to a specific switching state. When the reference vector lies within a particular region, the inverter directly applies the associated voltage vector without the need for interpolation or modulation. This natural selection mechanism significantly reduces the number of commutations, leading to substantially lower switching losses compared to modulated control methods.

However, a notable limitation of NVC arises from its inherently low and non-uniform switching frequency, which may result in the injection of low-order harmonics into the output voltage. This drawback can be mitigated by employing converters with a higher number of voltage levels-typically greater than seven-thereby increasing the density of the state-space and enabling finer vector approximation. As a result, THD can be effectively reduced [97].

Despite its structural simplicity, implementing NVC requires a real-time algorithm capable of determining the closest available vector to the instantaneous reference. Fortunately, the computational complexity of such algorithms remains relatively low, making NVC a viable and efficient solution for industrial applications where low switching losses and hardware simplicity are of primary importance [2].

3.3.2 High Switching Frequency Modulation

This section examines three principal modulation strategies. Each method will be analyzed in the following subsections with respect to its modulation principles and operational characteristics. One of the primary categories within this framework is multicarrier PWM, which encompasses techniques such as Phase Disposition, Phase Opposition Disposition, Alternative Phase Opposition Disposition, and Phase-Shifted PWM. Another significant strategy is SVM, which conceptualizes the inverter's voltage space as a vector in a two-dimensional complex plane. The final category consists of hybrid modulation techniques, which integrate elements of different modulation techniques, aiming to capitalize on the advantages of both approaches.

3.3.2.1 Multicarrier Pulse Width Modulation

Multicarrier PWM is a widely used high switching frequency technique in MLIs, where N_{level} - 1 triangular carrier signals are compared against a single sinusoidal

reference to generate the inverter's output voltage. The arrangement of these carriers relative to the reference waveform has a significant impact on the harmonic spectrum. Different disposition strategies aim to improve waveform quality and minimize harmonic content, particularly at the carrier frequency and its multiples [98].

Multicarrier PWM is broadly categorized into two primary techniques: Carrier Disposition and Phase Shifted PWM. The Carrier Disposition method is further subdivided into three distinct approaches: Phase Opposition Disposition, Phase Disposition, and Alternative Phase Opposition Disposition.

These methods are employed to optimize harmonic performance and output voltage quality by configuring the phase and amplitude relationships of carrier waves. Each technique is defined in the following subtitles.

Phase Disposition:

In Phase Disposition configuration, all triangular carriers are aligned in phase. This leads to a symmetric carrier layout. Each comparison with the reference signal yields discrete output voltage levels. Although the harmonic behavior of Phase Disposition is not extensively detailed in the original analysis, it serves as a fundamental basis for comparison among other techniques [98].

Phase Opposition Disposition:

Phase Opposition Disposition arrangement places all carriers above the zero reference in phase, while those below are 180° out of phase. This symmetry contributes to suppressing harmonics located around the carrier frequency. Analytical models demonstrate that Phase Opposition Disposition can reduce carrier-related harmonics and improve the quality of the output voltage waveform, especially in high-performance applications [98].

Alternative Phase Opposition Disposition:

Alternative Phase Opposition Disposition arranges carriers in alternating phase opposition-each successive carrier is phase-inverted with respect to the previous one. This approach is particularly effective in attenuating harmonics around the switching frequency. Alternative Phase Opposition Disposition maintains strong

harmonic suppression performance even at low modulation indices, making it a reliable choice for reducing EMI and improving spectral performance [98].

Phase-Shifted:

The Phase-Shifted strategy, especially suited for CHB inverters, introduces equal phase shifts between consecutive carriers. As a result, each H-bridge cell modulates independently, leading to a more distributed switching pattern. This not only improves harmonic dispersion but also simplifies filtering requirements by spreading the high-frequency components across the spectrum [98].

3.3.2.2 Space Vector Modulation

SVM is a PWM technique utilized for efficient control of voltage vectors in MLI systems. It is based on representing the three-phase system in a mathematical vector space, allowing phase-to-phase voltages to be modeled within a three-dimensional Euclidean vector framework. The core objective of SVM is to synthesize the reference voltage vector by combining the nearest available switching vectors to achieve the desired average voltage within a modulation cycle [2], [99].

Given that the number of switching states increases exponentially with the number of levels in MLIs, traditional SVM algorithms become computationally intensive for higher-level configurations. However, the fast SVM algorithm introduced by Celanovic and Boroyevich mitigates this complexity by employing transformation matrices and non-orthogonal coordinate systems (e.g., hexagonal coordinates). This method reduces the problem to two dimensions and identifies the three nearest switching vectors to the reference vector. Their corresponding duty cycles are then computed using basic arithmetic expressions, significantly enhancing computational efficiency.

This strategy not only ensures hardware independence but also allows the algorithm to be adapted for any n-level converter. Furthermore, its real-time implement ability on standard DSPs makes it particularly practical for industrial applications [99].

3.3.3 Hybrid Modulation Techniques

Hybrid modulation techniques are introduced as an efficient strategy to reduce switching losses and improve overall efficiency in MLIs composed of multiple cascaded cells (such as CHB structures) with unequal power ratings. In this

technique, the high-power cells are switched using low-frequency square wave patterns, while only the low-power cell operates with high-frequency PWM control (e.g., unipolar PWM). This selective use of switching frequency significantly minimizes system losses since high-frequency switching is confined to the smallest power device.

For instance, in a three-cell CHB inverter, the largest voltage cell is switched based on comparison with a threshold derived from the sum of the smaller DC sources. The output of this cell is subtracted from the overall reference signal, and the result becomes the reference for the next cell. This process is repeated, and the final error signal is modulated via high-frequency PWM by the lowest-power cell, thus reconstructing the desired voltage waveform with high accuracy and minimal harmonic content.

However, the successful implementation of this method depends on maintaining specific proportional relationships between the DC voltage sources of the cells, such as 1:2:6. Without such ratios, the smallest cell could enter an overmodulation condition, leading to unwanted distortion [2].

3.4 Application Areas of Multilevel Inverters

Given their superior harmonic performance, lower voltage stress on switches, and scalability, MLIs are also being increasingly investigated for applications where cost, control complexity, and component minimization remain critical design considerations [100]. This section addresses the application areas of MLIs. Specifically, the usage of this technology is examined under the headings of Renewable Energy Systems, EVs and Transportation Systems, HVDC Transmission and FACTS Devices, and Industrial Drives and Motor Control.

3.4.1 Renewable Energy Systems

The growing global demand for electrical energy, coupled with the depletion of fossil fuel reserves, necessitates more efficient utilization of existing energy resources. Consequently, there has been an accelerated shift towards renewable energy systems, driven by the imperative to minimize energy losses and enhance power quality. In this context, advanced power electronic technologies and effective control strategies have become crucial. Inverters, in particular, play a pivotal role by converting DC into AC, thus enabling the integration of solar and

wind power systems, grid synchronization, and bidirectional power flow control [40].

Among the various inverter topologies, MLIs have gained prominence as a viable solution for medium- and high-power renewable energy integration. They offer several advantages, such as lower THD, higher output voltage quality, and improved efficiency due to low switching frequencies. In grid-connected PV and wind power systems, MLIs contribute to enhanced system performance through their modular structure and capability to synthesize staircase waveforms from multiple DC sources. Furthermore, the development of RSC-MLI topologies has enabled cost-effective and compact designs, making them particularly suitable for large-scale renewable deployments. These advancements have made MLIs a critical enabler in transitioning toward sustainable and decentralized energy infrastructures [101], [102].

In recent years, the integration of renewable energy sources such as solar and wind has been significantly enhanced by the evolution of MLI technology, particularly those with RSC-MLI. These topologies address key challenges in renewable systems, including minimizing switching losses, managing voltage stress, and achieving high efficiency at low switching frequencies. RSC-MLIs are especially well-suited for PV and wind applications due to their ability to synthesize high-quality AC waveforms from multiple DC sources while utilizing fewer semiconductor components. This results in reduced cost, volume, and complexity-key advantages for large-scale deployments. Moreover, advanced control strategies such as SHE and carrier-based PWM have been successfully applied to RSC-MLIs, enabling compliance with grid codes like IEEE 519 through effective harmonic mitigation and voltage balancing. The combination of modular architecture, control flexibility, and improved power quality makes RSC-MLIs a highly promising solution for modern, distributed renewable energy networks [101].

Beyond the general advantages of MLI structures in renewable energy integration, recent research has proposed innovative topologies to further enhance efficiency and compliance with grid standards. One such development is a three-phase, grid-connected MLI based on a parallel structure of multiple two-level inverter legs, each fed by separate renewable energy sources such as PV arrays or wind turbines. This modular approach enables a scalable generation of high-quality multilevel

output waveforms with optimized THD, especially when using pulse width and height modulation strategies. The topology offers a high number of voltage levels - up to 2 x N_{leg}^2 - 2 - with significantly reduced switching frequency and component count compared to traditional topologies such as CHB inverters. Additionally, simulation and experimental results confirmed compliance with IEEE 519 and IEC 61000-3-12 standards, demonstrating excellent harmonic performance and low switching losses, making the proposed MLI topology an efficient and cost-effective solution for medium- to large-scale renewable energy grid integration [103].

3.4.2 Electric Vehicles and Transportation Systems

The electrification of transportation has become a central focus in global energy strategies, driven by the imperative to reduce greenhouse gas emissions and fossil fuel dependency. In this context, MLIs play a pivotal role in enabling efficient and scalable EV and hybrid EV technologies. Compared to traditional two-level inverters, MLIs offer superior waveform quality, reduced switching losses, lower EMI, and improved fault tolerance - all of which contribute to enhanced drive efficiency and system reliability [41], [104].

One of the most prominent multilevel topologies used in electric traction systems is the CHB inverter. Its modular design enables the synthesis of nearly sinusoidal waveforms with reduced harmonic distortion, even under low switching frequencies. According to Tolbert et al., an 11-level CHB inverter can achieve THD below 5% without any output filters, while significantly lowering EMI and voltage stress compared to conventional PWM drives. These features make CHB inverters ideal for large traction systems such as electric buses, trucks, and locomotives [104].

As EVs move toward higher voltage architectures (e.g., 800 V and above), MLIs allow the use of low-voltage-rated semiconductor switches to achieve high-voltage output, enhancing both safety and thermal performance. Vehicles like the Porsche Taycan and Lucid Air are adopting such systems to achieve better efficiency and power density. MLIs further support bidirectional power flow, which is essential for regenerative braking and fast charging [41].

A critical development in this field is the hybrid cascaded multilevel converter, designed specifically for battery energy management in EVs. As described by Yuan

et al., this topology enables selective charging/discharging of individual battery modules, achieving state-of-charge balancing without the need for external balancing circuits. Moreover, its modular architecture supports fault isolation-allowing the vehicle to continue operating even if certain battery cells or modules fail [105].

Another advancement is the CHB multilevel boost inverter proposed by Koohi-Kamali et al., which completely eliminates the need for inductors. This inverter relies on capacitive energy storage and a unique switching strategy to regulate capacitor voltages while producing a five-level phase voltage output. It demonstrates high power density and voltage boost capability from low-voltage DC sources-ideal for compact EV/ Hybrid EV platforms [106].

In summary, MLIs-particularly modular and hybrid topologies-are becoming foundational in the next generation of electric mobility. They not only improve drive efficiency and reliability but also integrate seamlessly with battery management and high-voltage architecture, enabling the future of clean, electrified transport.

3.4.3 HVDC Transmission and FACTS Devices

The increasing demand for flexible and reliable power transmission has significantly encouraged the use of HVDC systems and FACTS in modern power networks. While HVDC transmission is primarily applied to facilitate efficient long-distance power transfer and interconnection of asynchronous grids, FACTS devices are employed to enhance controllability, stability, and voltage regulation in AC networks.

FACTS controllers such as STATCOM, Static Synchronous Series Compensator, and Unified Power Flow Controller rely on high-power VSIs, which are crucial for reactive power compensation and dynamic voltage control. The implementation of these controllers often involves multilevel converter topologies due to their superior output quality, voltage scalability, and reduced harmonic distortion. Among these, modular designs like the chain (CHB), multipoint clamped, and nested-cell (like FC) converters provide varying trade-offs in terms of component count, transformer requirement, voltage control flexibility, and capacitor sizing requirements [108].

Notably, in distributed energy systems, particularly small-scale wind energy applications, FACTS functionalities can be integrated directly into MMCs. These designs enable the inverter to function both as a power converter and as a Distribution-STATCOM, allowing it to regulate the power factor without the need for external reactive compensation devices.This dual functionality leads to enhanced power quality and reduced system cost, especially when the reactive power is controlled independently via modulation index and active power via phase angle adjustment [109].

Moreover, voltage balancing within multilevel converters is vital for maintaining system stability, especially under low switching frequencies typical in large-scale FACTS applications. Advanced modulation techniques, such as triangular carrier PWM combined with harmonic injection, have been explored to ensure stable midpoint voltage across split DC capacitors in NPC inverters, thus making them suitable for reactive power-dominant FACTS operations [110].

HVDC transmission offers significant advantages over conventional AC systems in terms of efficiency and controllability, especially in long-distance energy transmission, interconnection of isolated networks, and integration of renewable resources. VSC-based HVDC technologies provide independent control of active and reactive power, fast dynamic response, reduced filtering requirements, and the ability to interface with weak grids-advantages not available in classical CSI HVDC systems [111].

MMCs, as an advanced topology in VSC-HVDC systems, enable high modularity, low switching losses, better harmonic performance, and scalability to high voltage levels. Each phase leg of an MMC typically includes hundreds of submodules, where each submodule contains capacitors and semiconductor switches such as IGBTs and diodes. This multilevel voltage waveform significantly reduces the filtering demand and enhances efficiency.

However, the detailed electromagnetic transient modeling of MMCs becomes computationally burdensome due to the high number of switching elements. Therefore, Average Value Models are employed to replicate the dynamic response of detailed models using controlled voltage and current sources rather than explicit semiconductor switching. These Average Value Models significantly reduce

simulation time while maintaining sufficient accuracy for system-level studies [112].

MMC-HVDC systems are widely used for the integration of offshore wind farms into onshore grids. However, internal dynamics such as capacitor voltage oscillations and circulating currents can lead to subsynchronous oscillations, especially under partial load conditions. In a practical MMC-HVDC project in China, subsynchronous oscillations in the range of 20-30 Hz were observed, resulting in system shutdowns triggered by protection mechanisms.

To analyze and mitigate such oscillations, impedance-based small-signal models of MMCs have been developed using Harmonic State-Space techniques. These models allow frequency-domain analysis of the MMC's time-varying behavior. Studies indicate that the conventional design approach-tuning the wind farm inverter and HVDC controller separately-is insufficient for ensuring system-wide stability. Instead, coordinated parameter optimization is required for both converter stations to effectively suppress the subsynchronous oscillation phenomenon [113].

3.4.4 Industrial Drives and Motor Control

In modern industrial environments, especially in sectors such as steel production, mining, and electric transportation, the need for high-performance motor drive systems has become increasingly critical. This is driven by demands for higher efficiency, compactness, and dynamic performance. MLI topologies play a central role in satisfying these requirements, particularly for medium- and high-voltage applications.

Initially, two-level inverters were widely employed due to their structural simplicity and cost-effectiveness. However, their limited output voltage and poor harmonic performance posed serious drawbacks when used in high-power industrial drives. In contrast, three-level NPC inverters emerged as an effective solution, offering enhanced waveform quality, reduced voltage stress, and better energy efficiency.

The application of three-level NPC inverters in rolling mills and liquefied natural gas compressors has demonstrated significant improvements in drive performance. Their efficiency, when combined with advanced power semiconductor devices can reach up to 99%. Additionally, five-level inverters have been proposed for ultra-

large drives (up to 120 MVA) to further improve voltage quality and reduce torque ripple in critical applications [114].

Furthermore, recent advancements in semiconductor technology have significantly contributed to the development of three-level NPC inverters. Industrial applications now widely adopt IGBTs and IGCTs, replacing traditional GTOs and enabling improved switching characteristics, higher efficiency, and snubber less operation. Moreover, the introduction of the ANPC topology has addressed the unequal loss distribution observed in conventional NPC designs, enhancing thermal stability and overall reliability in medium-voltage drives. These innovations have enabled three-level NPC inverters to dominate the medium-voltage converter market, particularly in applications such as oil and gas, mining, water treatment, and heavy industries, operating in voltage ranges from 2.3 kV to 4.2 kV and power capacities up to 16 MVA [115].

In parallel with these innovations, modular MLIs have emerged as another breakthrough for medium-voltage motor drives. This topology employs a stack of bidirectional chopper-cells to produce multilevel voltage waveforms, significantly reducing common-mode voltage and torque ripple. The distributed energy storage in floating DC capacitors allows flexible control strategies such as averaging and balancing, ensuring voltage stability across cells. Experimental studies on a 15-kW scaled prototype confirm that these inverters can operate at low switching frequencies while still achieving sinusoidal motor currents and minimizing EMI. Furthermore, modular MLIs are especially advantageous for variable-speed applications like fans, pumps, and blowers, offering improved efficiency and smoother torque profiles across medium-voltage ranges [116].

Building upon these advancements, a novel trinary hybrid 81-level inverter topology has recently been proposed, offering substantial benefits for motor drive applications. This inverter synthesizes 81 voltage levels per phase using a minimum number of components and eliminates common-mode voltage, a major source of EMI and bearing failures in traditional inverters. Its bidirectional DC-DC converters not only stabilize the DC-link voltages with high bandwidth control but also enable power to flow in both directions - a key feature under low modulation index conditions. With SVM operating at low switching frequencies and vector control for the motor, the topology ensures high dynamic performance, minimal

THD (as low as 1%), and near-linear modulation characteristics. These features make it highly suitable for high-performance and energy-efficient motor drives in future industrial applications [117].

Haruna et al. proposed an innovative three-level twin-drive inverter architecture that can independently control two Permanent Magnet Synchronous Motors while requiring fewer switches (21 instead of 24) and eliminating the need for 12 diodes used in conventional designs. This topology integrates features from both three-level NPC and 9-switch inverters, offering better performance and reduced size and cost, making it particularly suitable for EVs and Hybrid EVs [118].

In addition, Sekhar and Das introduced a four-level inverter configuration formed by cascading three two-level inverters. This topology enables the generation of 512 space vector combinations and eliminates neutral point voltage fluctuations. Compared to traditional four-level inverters or CHB configurations, it uses fewer power devices and requires fewer isolated power supplies. Moreover, both SVM and multilevel carrier-based PWM techniques are effectively utilized to improve the quality of output voltages [119].

In modern industrial motor control systems, the choice between VSIs and load-commutated inverters plays a crucial role in addressing high-power applications exceeding 20 MW, such as large compressors and synchronous motor drives. VSI-based drives offer enhanced flexibility, allowing operation with both synchronous and induction machines, and providing high power factor performance (>0.95) through diode or active front-end rectifiers without the need for external compensation. Their modular structures and multilevel configurations, including CHB and MMCs, enable low harmonic distortion and high dynamic response, particularly advantageous for applications requiring wide frequency variation and long cable distances. However, load-commutated inverters retain a competitive edge in system reliability and scalability, mainly due to their simple thyristor-based topology, which enables robust fault handling and higher power scalability without requiring parallel converters. Field experience confirms that load-commutated inverters can sustain operation during deep voltage dips and offer partial torque generation down to 50% of rated voltage, outperforming VSI systems in fault ride-through capability. Furthermore, press-pack semiconductors such as IGCTs and Press-Pack Controlled Thyristors are favored for both load-commutated inverters

and VSI implementations due to their arc-flash safety and low conduction losses, contributing to high overall system efficiency and reliability in industrial environments [120].

In conclusion, transitioning from two-level to advanced MLIs has revolutionized industrial motor control, enabling higher voltage operation, lower harmonic distortion, and better energy utilization. These advancements are crucial for both technical performance and environmental sustainability in modern industry [114], [118], [119].

3.4.5 Smart Grids and Distributed Generation

The increasing integration of smart grids and distributed generation has propelled the adoption of voltage source MLIs as core components in advanced microgrid architectures. Among these, CHB MLIs play a pivotal role within Solid-State Transformers, which replace traditional line-frequency transformers by offering intelligent functionalities such as power flow control, voltage regulation, harmonic isolation, and bidirectional energy transfer. CHB-based Solid-State Transformers enable the connection of low-voltage (400 V) renewable energy sources to medium-voltage (10 kV) distribution systems through a Dual Active Bridge stage that provides high-frequency galvanic isolation and voltage boosting. While the modular nature of CHB inverters facilitates high-quality output with reduced THD, they are also prone to per-phase and per-module power and voltage imbalances. To mitigate these issues, the paper proposes an advanced control framework that includes zero-sequence voltage injection for phase balancing and a feedforward control mechanism to maintain DC-link voltage uniformity across modules. These innovations significantly enhance the performance, reliability, and scalability of Solid-State Transformers-based microgrid systems, making them highly suitable for integrating distributed renewable energy sources into smart grid infrastructures [121].

The implementation of MLIs, particularly those employing wide-bandgap semiconductors such as gallium nitride (GaN) field-effect transistors, has demonstrated significant efficiency benefits in low-voltage drive systems. Among the evaluated configurations, the five-level GaN-based inverter operated at 20 kHz provides the most advantageous compromise between system complexity and

energy efficiency. While increasing the number of levels beyond five-such as in seven-level topologies-can offer marginal improvements in total system losses (3% at 25 °C, 5% at 150 °C), the associated increase in circuit complexity and component count is rarely justified. In practical terms, the five-level GaN-based inverter achieves up to 60% and 63% loss reduction in inverter and filter components at 25 °C and 150 °C, respectively, when compared to a conventional two-level IGBT-based inverter. These reductions not only enhance overall system efficiency but also enable reductions in filter size and cooling requirements, making the five-level GaN inverter a viable solution for compact, high-efficiency drive systems in industrial applications. As such, MLI technology continues to evolve as a key enabler of future-oriented, energy-efficient power conversion systems in both emerging and established industrial sectors [122].

In conclusion, MLIs are widely utilized in various applications ranging from renewable energy systems (such as solar and wind), EVs and transportation networks, to HVDC transmission lines, FACTS devices, and industrial motor drives. Owing to their high efficiency, low harmonic distortion, enhanced power quality, and system flexibility, they have become an essential component of modern power systems.

4
PROPOSED ASYMMETRIC TWENTY-ONE LEVEL INVERTER TOPOLOGY AND CONTROL STRATEGY

This chapter introduces a novel asymmetric twenty-one level inverter topology specifically designed to enhance voltage resolution while reducing the number of components, switching losses, and control complexity. As MLI technologies continue to evolve to meet the demands of high-performance power conversion, the development of asymmetrical configurations offers a promising path toward achieving a better trade-off between circuit efficiency, cost, and harmonic performance. The proposed topology emphasizes optimized voltage source utilization and strategic modulation design to generate a high-quality stepped output waveform with minimized THD.

The chapter is organized to first outline the key design objectives and original contributions of this work, followed by a comprehensive presentation of the proposed circuit configuration. Attention is then directed to voltage source assignment schemes, detailing the appropriate DC source distribution needed to realize all twenty-one voltage levels. Furthermore, the selected modulation strategy is elaborated with a focus on switching pattern generation and harmonic control. Finally, voltage level derivation methods and corresponding switching sequences are presented in detail to demonstrate the inverter's ability to synthesize the desired output spectrum efficiently under both steady-state and dynamic load conditions.

4.1 Design Objectives and Contribution

This chapter focuses on the development and technical assessment of a novel asymmetric twenty-one-level inverter topology, emphasizing structural innovation and modulation strategy. The primary objective is to design a MLI configuration that achieves high-resolution output voltage levels using a reduced number of switches and simplified circuitry, thereby improving overall system efficiency and reducing implementation complexity.

MLI topologies have undergone continuous evolution in response to emerging demands in power electronics. Among them, RSC-MLIs have received significant

attention due to their potential to synthesize high-voltage waveforms using fewer semiconductor components. According to Li and Li [123], the future development of MLIs is guided by four main directions. The first involves the design of new converter topologies. While classical structures serve well for specific applications, there is a growing need for customized and modular topologies suited to diverse voltage and frequency requirements. In this regard, hybrid configurations-such as those combining elements of ANPC, FC, and MMC-are gaining prominence. Secondly, the integration of wide bandgap semiconductors, especially SiC and GaN devices, is anticipated to revolutionize MLI design by enabling higher switching frequencies, lower losses, and more compact converter architectures. Third, the application scope of MLIs is expanding into emerging fields like electric mobility, energy storage, and solid-state transformers, which demand reliable, scalable, and component-efficient designs. Lastly, advanced modulation and control techniques will play a crucial role in reducing harmonic distortion and ensuring voltage balancing-especially through efficient utilization of redundant switching states [123]. Looking ahead, widespread adoption of hybrid MLI architectures and integration of artificial intelligence-based control and modulation algorithms-such as genetic algorithms or particle swarm optimization for SHE- are expected to define future research. These techniques offer the potential to reduce switching losses and improve harmonic profiles significantly [124]. Additionally, the lack of standardized metrics for evaluating and comparing different MLI topologies impedes objective performance assessment and classification [125].

The proposed topology employs asymmetrical DC voltage sources in a strategically arranged configuration to generate twenty-one discrete voltage levels. A key design goal is to exploit the unequal magnitude of DC sources to maximize the number of voltage levels while minimizing the number of required power switches and gate drivers. This approach leads to a compact and cost-efficient inverter structure suitable for applications where space, cost, and performance are critical considerations.

To control the switching of power devices, the NLC strategy is implemented. This modulation technique is chosen for its simplicity, effectiveness in minimizing THD, and its ability to reduce switching losses by operating at fundamental frequency. Through this strategy, the proposed inverter achieves high-quality output

waveforms with improved harmonic performance, while maintaining a low switching frequency, which is beneficial for thermal management and device longevity.

In summary, the key contributions of this chapter include:

- The design of a novel asymmetric inverter topology capable of generating twenty-one voltage levels using fewer switches than conventional multilevel structures.
- A systematic configuration of asymmetric DC sources to enable efficient voltage level generation with minimal hardware.
- The implementation of an NLC switching scheme to reduce THD and switching losses.
- A detailed methodology for voltage level derivation based on the combination of unequal DC sources, enabling precise synthesis of multilevel output waveforms.

These contributions collectively support the development of a scalable and efficient inverter solution that advances MLI technology in terms of both design simplicity and performance.

4.2 Circuit Configuration

The proposed asymmetric twenty-one-level inverter topology adopts a functionally structured and optimized arrangement consisting of an H-bridge and auxiliary switching elements. This configuration significantly reduces the total number of switching components while enabling the generation of a high-resolution output waveform, thereby minimizing system size, complexity, and cost.

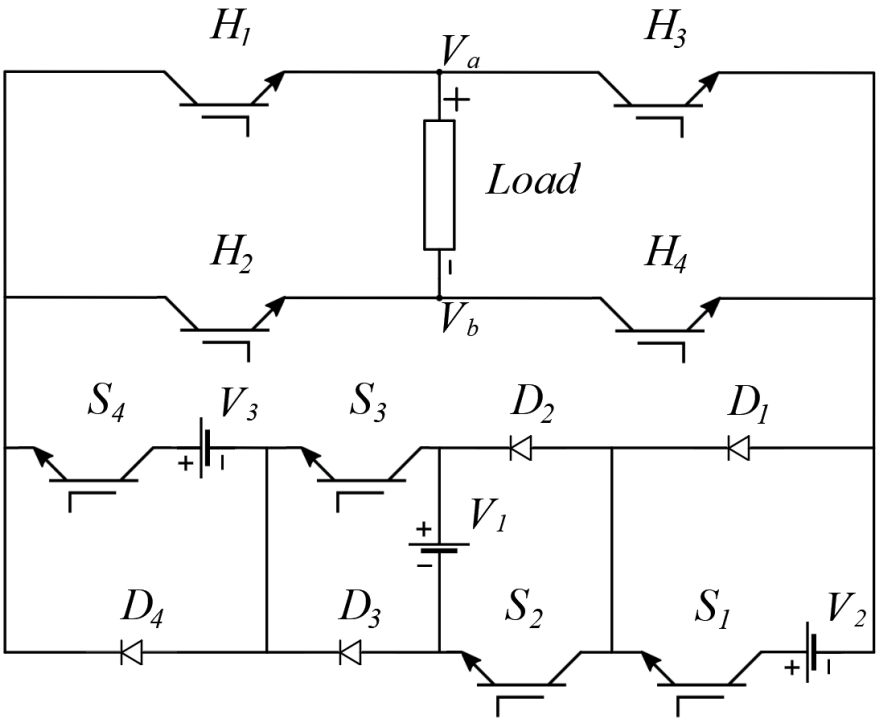


Figure 4.1 The structure of the asymmetrical twenty-one-level MLI topology

Figure 4.1 illustrates the structural configuration of the proposed asymmetric twenty-one-level MLI topology. It visually represents the component arrangement and the voltage level generation logic underlying the proposed system.

The circuit incorporates three asymmetrical DC voltage sources ($V_1 = V_{dc}$, $V_2 = 3V_{dc}$, $V_3 = 6\ V_{dc}$) strategically combined through four main switches (S_1-S_4) to generate twenty-one distinct output voltage levels. Proper sequencing of these sources allows for the generation of both positive and negative voltage levels. The polarity reversal is achieved using a conventional H-bridge composed of four switches (H_1-H_4), which controls the direction of current through the load and enables bipolar output waveform generation.

The circuit includes four diodes (D_1-D_4) to ensure safe and reliable operation. Diodes D_1 and D_4 allow continuous current flow when the voltage sources they are connected across are deactivated, preventing abrupt current interruptions. Diodes D_2 and D_3 operate in coordination with switches S_2 and S_3, enabling the V_1 source to be utilized in both positive and negative polarities. This design enhances switching safety and supports stable transitions between voltage levels.

The proposed MLI topology is fundamentally composed of two primary structural blocks: the polarization unit and the level generation units (See Figure 4.2 - The Fundamental Units of the Proposed MLI Topology). This architectural segmentation allows for a modular and systematic analysis, wherein the functionality and contribution of each sub-unit can be distinctly characterized.

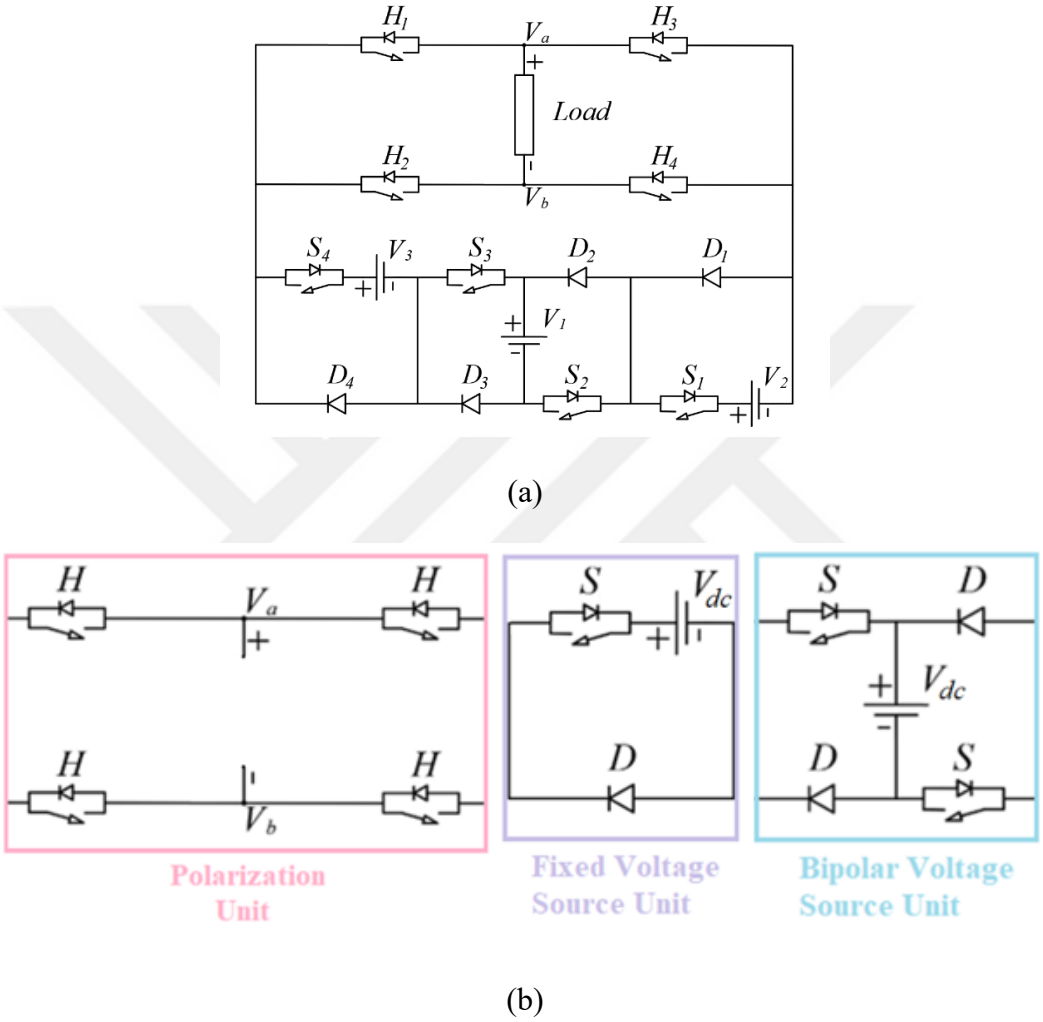


Figure 4.2 (a) The basic structure of the asymmetrical twenty-one-level MLI topology (b) the fundamental units of the proposed MLI topology

The polarization unit, implemented through an H-bridge circuit, determines whether the voltage level generated by the level generation units will appear as a positive or negative value at the output. This unit ensures the bipolar nature of the output voltage, thereby enabling AC generation.

The level generation units consist of two distinct substructures:

- Bipolar Voltage Source Unit (BVSU)

- Fixed Voltage Source Unit (FVSU)

The FVSU incorporates a fixed positive DC voltage source and contributes exclusively to the generation of positive voltage levels at the output. This unit provides unipolar voltage steps that remain constant over time.

In contrast, the BVSU includes a bipolar DC source that can generate either a positive or a negative voltage depending on the switching sequence at different time intervals. This enables the BVSU to contribute with either polarity, depending on the required output voltage level.

One of the key innovations of the proposed design lies in its ability to generate a high number of output levels using a reduced number of switching devices via an asymmetric voltage configuration. In the presented topology, two FVSUs and one BVSU are utilized, each associated with distinct DC voltage magnitudes. Through the appropriate sequencing of the switches and the strategic selection of voltage source amplitudes, a 21-level output waveform is successfully synthesized.

This asymmetric and reduced switch count configuration significantly lowers the number of power electronic components, gate driver circuits, and associated control complexity, while simultaneously achieving high-quality output voltage with improved resolution. The resulting structure offers enhanced efficiency, compactness, and scalability, making it highly suitable for applications in renewable energy systems, medium-voltage drives, and grid-connected converters.

4.3 Voltage Source Assignment

This section provides a detailed explanation of the assignment of DC voltage sources used in the proposed twenty-one-level asymmetric inverter topology and their roles in the generation of output voltage levels. The topology employs three DC voltage sources of unequal magnitudes: $V_1 = V_{dc}$, $V_2 = 3V_{dc}$, and $V_3 = 6V_{dc}$. These sources are combined in a specific logical configuration to generate a total of twenty-one distinct output voltage levels; each formed through appropriate switching combinations.

The primary reason for adopting asymmetric voltage sources instead of symmetric ones lies in the ability to produce a higher number of voltage levels while significantly reducing the number of power switches, diodes, and gate drivers required. In symmetric topologies, identical voltage sources are used, which leads

to an exponential increase in the number of components needed to achieve a given number of output levels. This results in increased system cost, complexity, and physical size.

In contrast, the asymmetric configuration allows for the use of different voltage magnitudes, enabling the generation of a high-resolution output waveform with fewer switching elements. This not only improves the system's harmonic performance by lowering THD but also enhances its overall efficiency. Moreover, the proposed structure is well-suited for implementation with NLC, as each voltage level is predefined and can be directly mapped through level selection.

In summary, the assignment of asymmetric voltage sources in the proposed topology is a deliberate strategy to maximize structural efficiency and operational performance. This design approach enables the development of a compact, cost-effective, and application-ready inverter capable of producing high-quality output with a minimal component count.

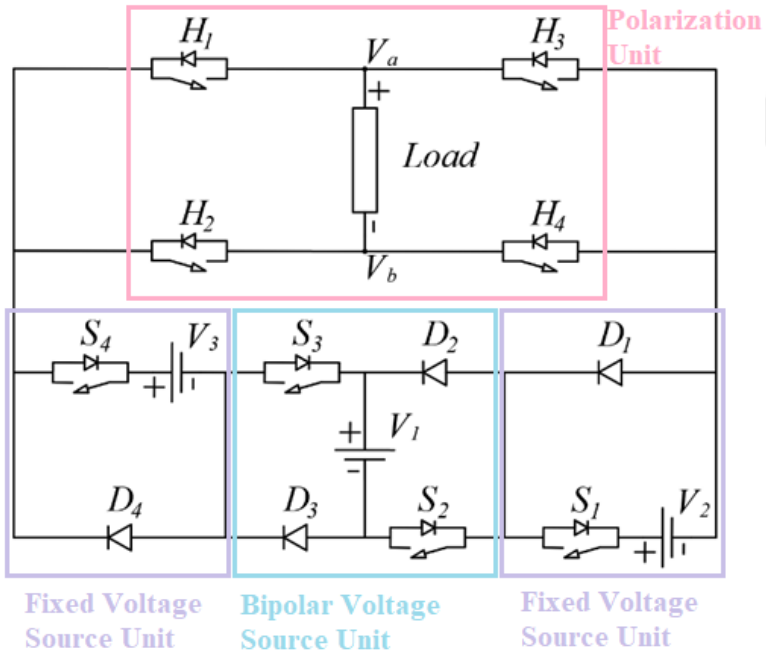


Figure 4.1 The units of the asymmetrical twenty-one-level MLI topology

The magnitudes of the voltage sources are designed according to specific scaling principles with the aim of achieving the target maximum number of output voltage levels using a minimal number of components and with maximum structural efficiency. This scaling strategy not only reduces hardware complexity but also facilitates the generation of high-resolution output voltage with low harmonic

distortion and a waveform closely approximating an ideal sinusoidal form. As a result, significant improvements are achieved in both system cost and key performance metrics such as THD. The overall configuration of these voltage sources within the proposed topology, along with the module types in which they are embedded, is clearly illustrated in Figure 4.3, which shows the arrangement of the Voltage Source Units used in the asymmetrical twenty-one-level MLI topology.

During this design process, the type of modules in which the voltage sources are embedded-referred to as voltage source units-plays a decisive role. In the proposed structure, the voltage sources are configured within one BVSU and two FVSUs. Each module type imposes its own internal scaling rules for defining the magnitude of the voltage sources it contains, thereby directly influencing the operating logic of the inverter's output voltage generation.

If a voltage source is located within a BVSU, the magnitude of the next voltage source to be integrated into the topology can be defined as three times that of the source already in the BVSU. This scaling rule allows a greater number of output voltage levels to be generated with fewer switching components compared to classical symmetric approaches. Consequently, the output waveform consists of more finely spaced discrete voltage levels, leading to a smoother, more continuous signal that more closely resembles a sine wave. As a result, the THD is significantly reduced, and the need for output filtering is minimized.

Similarly, if a voltage source is embedded within an FVSU, the magnitude of the next voltage source is defined as twice the value of the existing source in the same FVSU. This configuration increases the design flexibility of asymmetric structures and enables a wider range of feasible combinations within the overall inverter architecture.

In the proposed topology, the voltage source magnitudes are defined as $V_1 = V_{dc}$, $V_2 = 3V_{dc}$, and $V_3 = 6V_{dc}$. The first source, V_1, is placed within a BVSU, and therefore, the subsequent source V_2 is defined to be three times larger than V_1, resulting in $3V_{dc}$. Since V_2 is assigned to a FVSU, the next source, V_3, is selected to be twice the magnitude of V_2, yielding $6V_{dc}$. This hierarchical scaling structure enables the generation of twenty-one distinct output voltage levels using only three asymmetric voltage sources. Consequently, topology achieves high-quality output

voltage synthesis while maintaining a simplified structure and enhanced harmonic performance.

This scaling approach, like those proposed in the literature for asymmetric MLI topologies, contributes to reducing both the number of switching elements and the number of DC sources required. Moreover, it positions the proposed topology as an effective solution for practical applications where constraints such as size, cost, and efficiency are critical, particularly in renewable energy systems, EV drives, and medium-voltage industrial applications.

4.4 Modulation Strategy

To ensure high-quality voltage synthesis and optimal harmonic performance in MLIs, the selection of an appropriate modulation technique is of critical importance. The NLC technique is a widely adopted modulation strategy in MLIs, aimed at approximating a reference waveform by selecting the closest available discrete voltage level. This minimizes the deviation between the reference and the actual output voltage. Unlike PWM, which typically necessitates high switching frequencies, NLC operates with significantly reduced switching activity. This reduction not only decreases switching losses but also enhances the inverter's overall efficiency. Due to its computational simplicity and its ability to produce low harmonic distortion, NLC is particularly advantageous in applications requiring high power quality and efficiency.

Several variants of the NLC strategy exist for determining switching angles in MLIs. These include the Equal Phase method, Half-Equal Phase method, Half-Height method, and Feed-Forward method. Each variant offers a unique approach to approximating the reference sinusoidal waveform. The Equal Phase method uniformly distributes switching angles across the entire cycle, while the Half-Equal Phase method confines this distribution to half of the cycle to enhance waveform symmetry. The Feed-Forward method aims to minimize discontinuities in the waveform. However, the Half-Height method demonstrates superior harmonic performance by aligning switching transitions with the natural progression of the sinusoidal waveform.

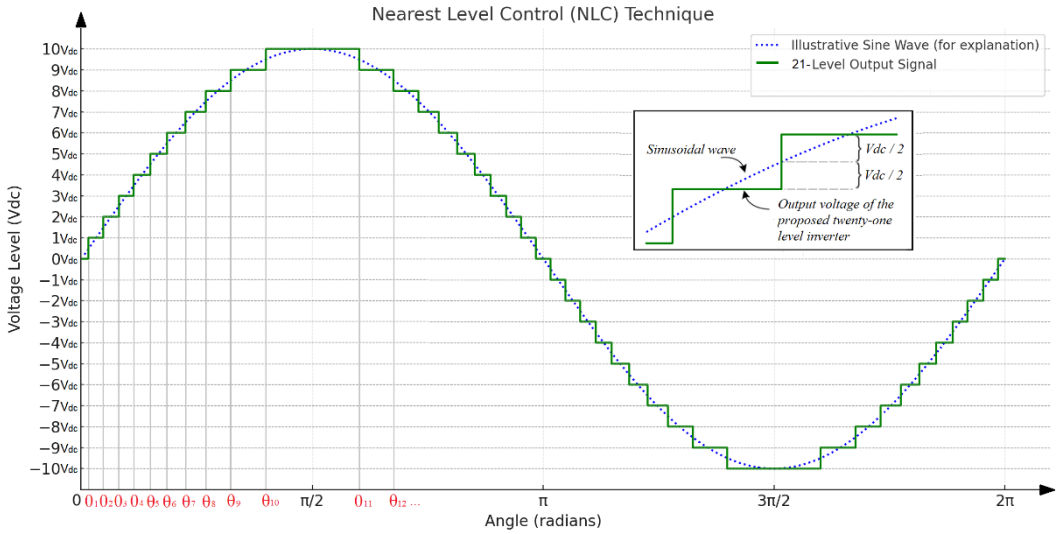


Figure 4.1 NLC based modulation scheme for proposed twenty-one-level MLI

The Half-Height method generates switching signals by tracking the sinusoidal reference voltage and identifying the midpoint between two successive voltage levels. A transition is triggered when the reference waveform intersects this midpoint, activating the appropriate switches to step to the next voltage level. As illustrated in Figure 4.4, which demonstrates the operational principle of the NLC technique, this synchronization ensures that the output waveform closely matches the reference sine wave, effectively reducing THD and improving overall power quality. By aligning the switching events with these half-height points, the Half-Height method ensures accurate and efficient waveform synthesis.

The following formula(4.1) is used to determine the switching angles (θ_i) for a 21-level inverter:

$$\theta_i = sin^{(-1)}((2i-1)/(N_{level}-1)) where, i = 1,2,3...((N_{level}-1)/2) (4.1)$$

The number of angles given N_{level} = 21 is N_{level} - 1 / 2 = 10. The switching angles are calculated by substituting i = 1, 2, 3, ..., 10 as follows:

$$\theta_1 = sin^{(-1)}((2-1)/(21-1)) \approx 2.87°$$

$$\theta_2 = sin^{(-1)}((2\times(2)-1)/(21-1)) \approx 8.63°$$

$$\theta_3 = sin^{(-1)}((2\times(3)-1)/(21-1)) \approx 14.48°$$

$$\theta_4 = sin^{(-1)}((2\times(4)-1)/(21-1)) \approx 20.49°$$

…

The switching angles corresponding to a twenty-one-level inverter are determined based on the Half-Height method, which leverages the symmetry of the sinusoidal waveform. For a full-cycle modulation scheme, these angles are computed across both the positive and negative half-cycles by exploiting the mirror symmetry and periodicity of the sine function. Accordingly, the calculated switching angles are approximately: 26.74°, 33.37°, 40.54°, 48.59°, 58.21°, 71.81°, 108.19°, 121.79°, 131.41°, 139.46°, 146.63°, 153.26°, 159.51°, 165.52°, 171.37°, 177.13°, 182.87°, 188.63°, 194.48°, 200.49°, 206.74°, 213.37°, 220.54°, 228.59°, 238.21°, 251.81°, 288.19°, 301.79°, 311.41°, 319.46°, 326.63°, 333.26°, 339.51°, 345.52°, 351.37°, and 357.13°.

These angles represent the precise transition points between discrete voltage levels, ensuring accurate approximation of the reference sinusoidal waveform and contributing to minimizing THD in the inverter output [59], [60], [126].

4.5 Voltage Level Derivation and Switching Schemes

In MLI systems, the generation of discrete output voltage levels through appropriate switching strategies is critical to achieving high-quality sinusoidal waveforms and minimizing harmonic distortion. The efficiency and performance of the inverter strongly depend on the configuration of DC voltage sources and the logic governing the switching states of the power semiconductor devices. This section presents a comprehensive analysis of the voltage level derivation process employed in the proposed twenty-one-level inverter topology, which utilizes asymmetrically scaled DC sources. Furthermore, detailed switching schemes corresponding to each voltage level are outlined to demonstrate how the desired output waveform is synthesized. The systematic arrangement of switching states not only ensures optimal component utilization but also contributes to reducing circuit complexity, switching losses, and overall system cost.

In the proposed inverter configuration, the magnitudes of the asymmetric DC voltage sources are selected to follow a special progression, thereby enabling a structurally efficient design with optimal utilization of components. The output voltage (V_{out}) levels are synthesized by strategically combining the DC sources (V_1, V_2, V_3) through defined switching states. The complete set of output voltage levels

generated by the proposed twenty-one-level MLI topology, along with the corresponding switching modes responsible for their realization, is comprehensively presented in Table 4.1. This table delineates the operational configurations that facilitate accurate voltage level synthesis.

TABLE 4.1: Operational modes of the proposed twenty-one-level MLI topology

Modes of operation	**S_1**	**S_2**	**S_3**	**S_4**	**H_1**	**H_2**	**H_3**	**H_4**	**Source combination**	**V_{out}**
Mode 10 (+)	1	1	1	1	1	0	0	1	$V_1+ V_2 + V_3$	$+10V_{dc}$
Mode 9 (+)	1	0	1	1	1	0	0	1	$V_2 + V_3$	$+9V_{dc}$
Mode 8 (+)	1	0	0	1	1	0	0	1	$V_2 + V_3 - V_1$	$+8V_{dc}$
Mode 7 (+)	0	1	1	1	1	0	0	1	$V_1+ V_3$	$+7V_{dc}$
Mode 6 (+)	0	1	0	1	1	0	0	1	V_3	$+6V_{dc}$
Mode 5 (+)	0	0	0	1	1	0	0	1	$V_3 - V_1$	$+5V_{dc}$
Mode 4 (+)	1	1	1	0	1	0	0	1	$V_1+ V_2$	$+4V_{dc}$
Mode 3 (+)	1	1	0	0	1	0	0	1	V_2	$+3V_{dc}$
Mode 2 (+)	1	0	0	0	1	0	0	1	$V_2 - V_1$	$+2V_{dc}$
Mode 1 (+)	0	1	1	0	1	0	0	1	V_1	$+1V_{dc}$
Mode 0 (I)	0	0	0	0	1	1	0	0	-	$0V_{dc}$
Mode 0 (II)	0	0	0	0	0	0	1	1	-	$0V_{dc}$
Mode 1 (-)	0	1	1	0	0	1	1	0	$-(V_1)$	$-1V_{dc}$
Mode 2 (-)	1	0	0	0	0	1	1	0	$-(V_2 - V_1)$	$-2V_{dc}$
Mode 3 (-)	1	1	0	0	0	1	1	0	$-(V_2)$	$-3V_{dc}$
Mode 4 (-)	1	1	1	0	0	1	1	0	$-(V_1+ V_2)$	$-4V_{dc}$
Mode 5 (-)	0	0	0	1	0	1	1	0	$-(V_3 - V_1)$	$-5V_{dc}$
Mode 6 (-)	0	1	0	1	0	1	1	0	$-(V_3)$	$-6V_{dc}$
Mode 7 (-)	0	1	1	1	0	1	1	0	$-(V_1+ V_3)$	$-7V_{dc}$
Mode 8 (-)	1	0	0	1	0	1	1	0	$-(V_2 + V_3 - V_1)$	$-8V_{dc}$
Mode 9 (-)	1	0	1	1	0	1	1	0	$-(V_2 + V_3)$	$-9V_{dc}$
Mode 10 (-)	1	1	1	1	0	1	1	0	$-(V_1+ V_2 + V_3)$	$-10V_{dc}$

Table 4.1 presents the switching states of the switches, where the binary values 1 and 0 represent the on and off states, respectively. This table is fundamental in illustrating the operational logic of the system under study and provides a clear representation of the control sequences applied.

The proposed twenty-one-level MLI topology achieves its high-resolution output by strategically configuring asymmetric DC voltage sources in combination with

precisely defined switching states. As illustrated in Table 4.1, each discrete output voltage level is synthesized through unique operating modes that determine the conduction state of power switches corresponding to each voltage source unit. These switching combinations enable the inverter to generate a wide range of output levels using a minimal number of components, thereby enhancing efficiency and reducing circuit complexity.

Table 4.1 provides a comprehensive overview of the operating modes necessary for generating all positive and negative voltage levels as well as the zero level. By coordinating the conduction paths across the asymmetric sources $V_1=V_{dc}$, $V_2=3V_{dc}$, and $V_3=6V_{dc}$, the inverter can deliver output voltages ranging from $-10V_{dc}$ to $+10V_{dc}$ in discrete steps.

This structured approach to switching state assignment ensures not only accurate voltage level synthesis but also contributes to the minimization of switching transitions per cycle, which in turn reduces switching losses and improves the thermal performance of the system. As such, Table 4.1 serves as a key reference for understanding the operational dynamics and control logic of the proposed MLI structure.

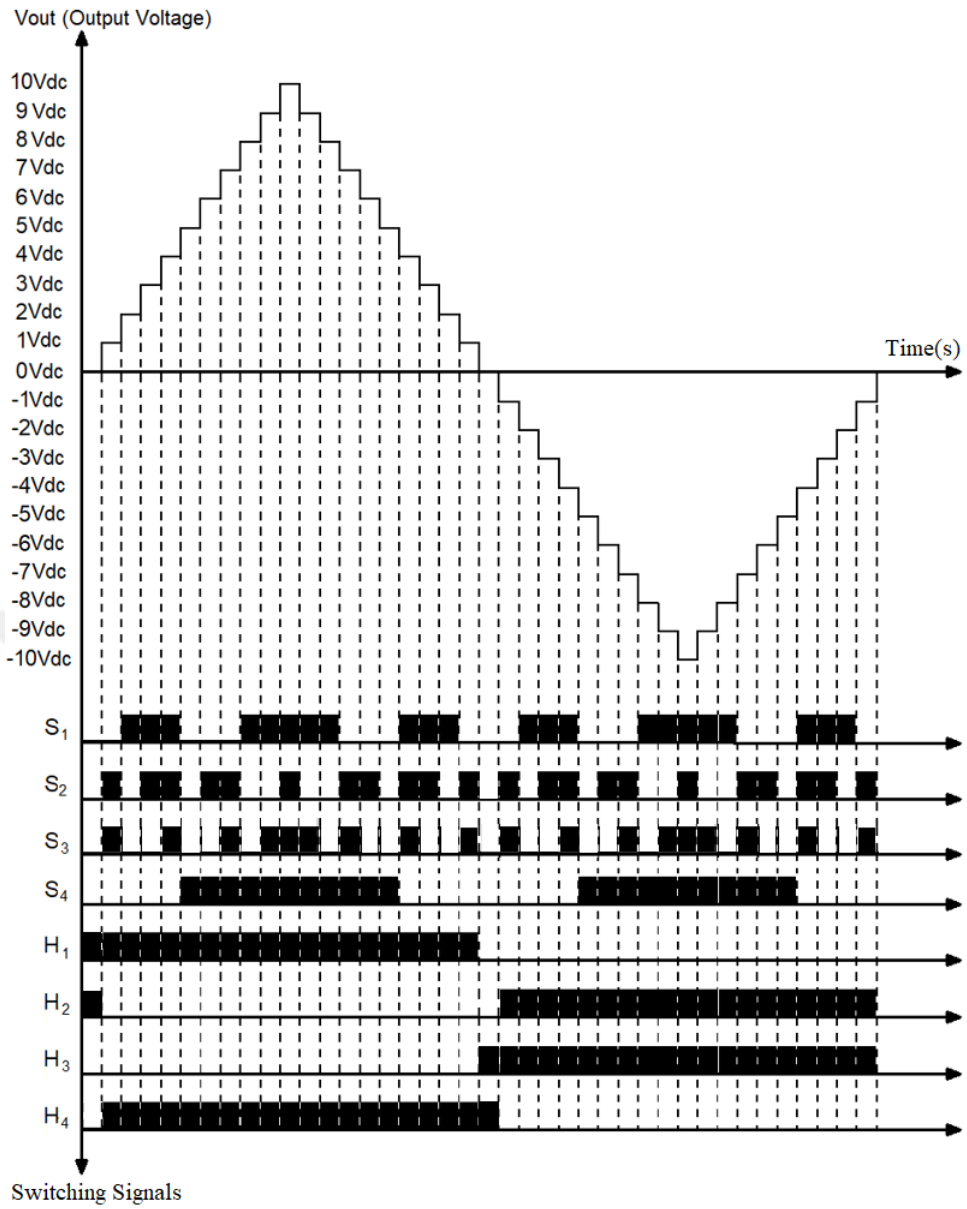


Figure 4.1 Voltage levels of the asymmetrical twenty-one-level MLI topology with a switching signal

Figure 4.5 illustrates the voltage levels generated by the asymmetrical twenty-one-level MLI topology in response to the applied switching signals. As shown in the figure, the topology successfully synthesizes twenty-one distinct output voltage levels by appropriately combining different DC voltage sources and controlling the switching devices accordingly. This figure demonstrates the effective modulation of the output waveform, confirming the accuracy and efficiency of the proposed switching strategy.

The fundamental function of MLIs is to generate a stepped output voltage waveform by appropriately combining voltage levels derived from DC sources V_1, V_2, and V_3. In the twenty-one-level inverter topology, the output voltage is determined by a variety of operating modes, each defined by a specific combination of switching states and source connections. These modes are classified into positive and negative voltage levels, depending on the polarity of the generated output voltage, with each mode corresponding to a unique configuration of conducting switches that guide the load current through the inverter circuit.

In the following sections, the switching sequences and corresponding source configurations associated with each operating mode are presented in detail, systematically outlining the progression of switching operations throughout the twenty-one-level inverter's functioning.

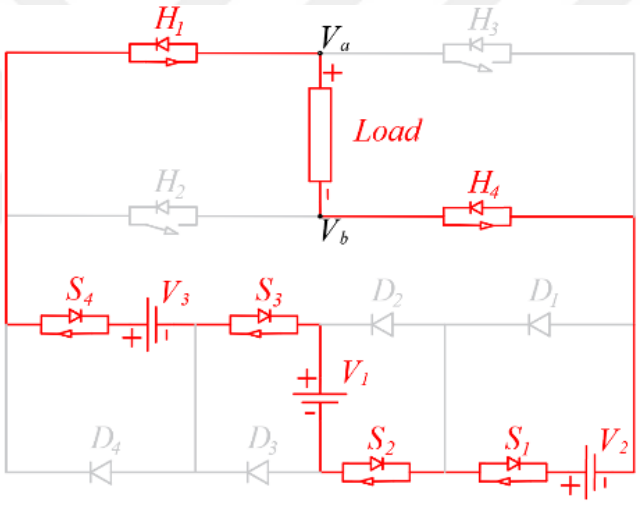


Figure 4.2 Mode 10 (+) - generation of $+10V_{dc}$ output voltage

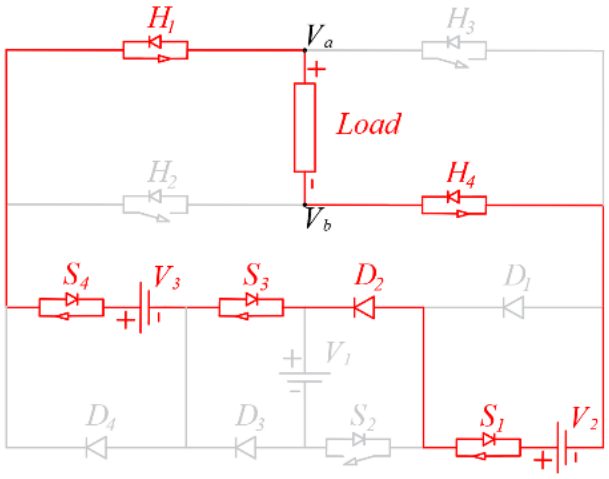


Figure 4.3 Mode 9 (+) - generation of +9V_{dc} output voltage

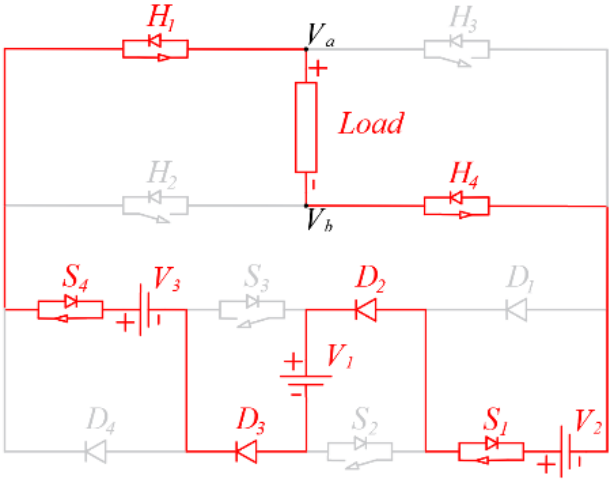


Figure 4.4 Mode 8 (+) - generation of +8V_{dc} output voltage

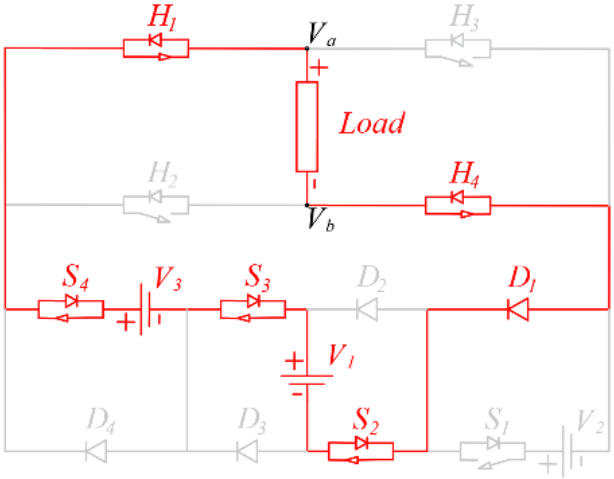


Figure 4.5 Mode 7 (+) - generation of +7V_{dc} output voltage

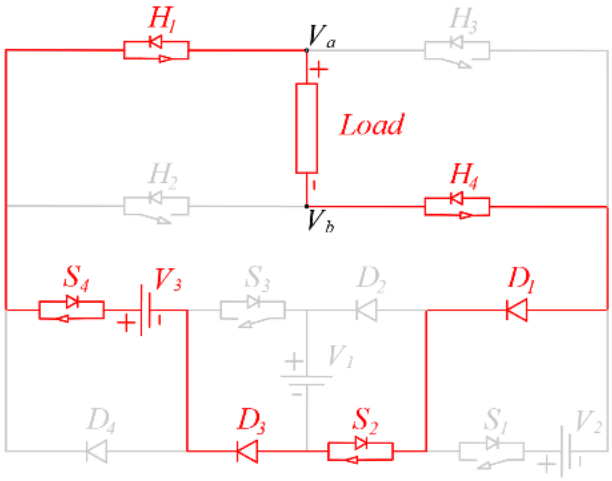


Figure 4.6 Mode 6 (+) - generation of +6V_{dc} output voltage

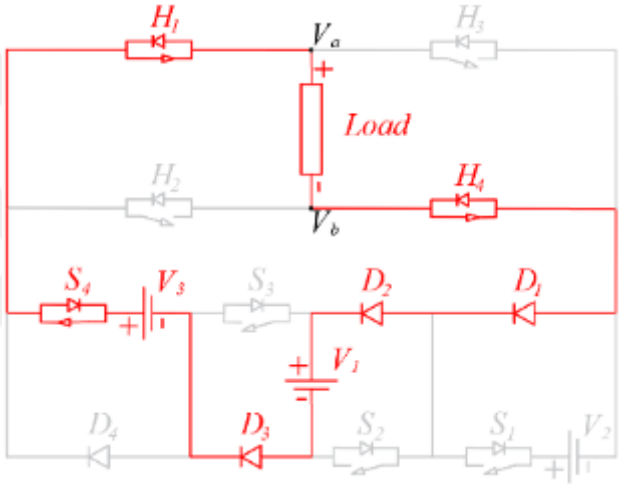


Figure 4.7 Mode 5 (+) - generation of +5V_{dc} output voltage

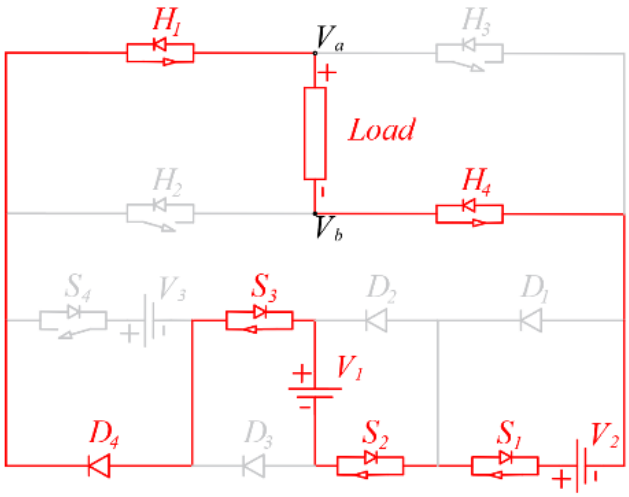


Figure 4.8 Mode 4 (+) - generation of +4V_{dc} output voltage

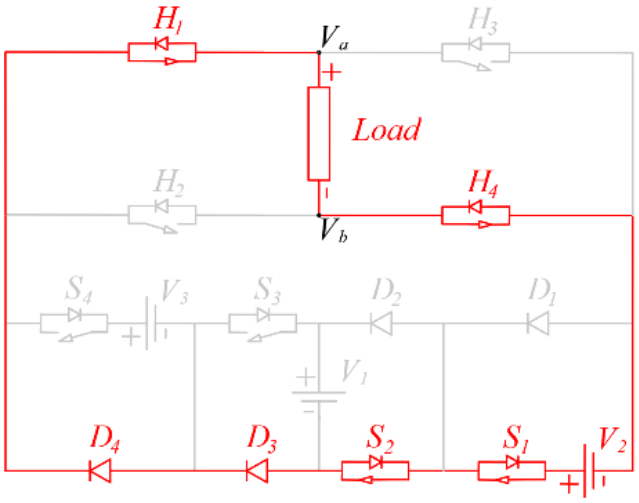


Figure 4.9 Mode 3 (+) - generation of $+3V_{dc}$ output voltage

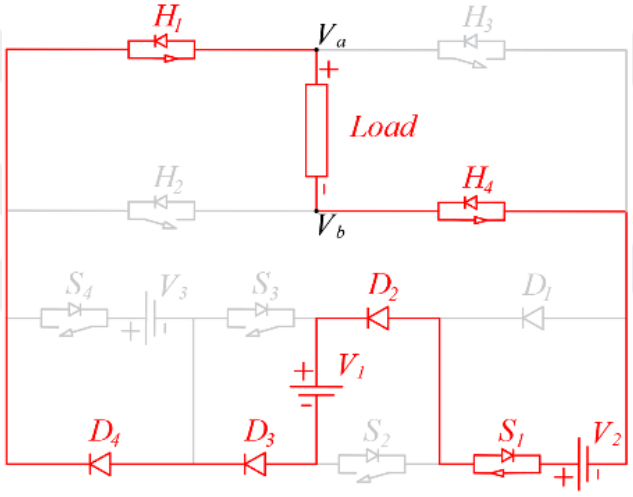


Figure 4.10 Mode 2 (+) - generation of $+2V_{dc}$ output voltage

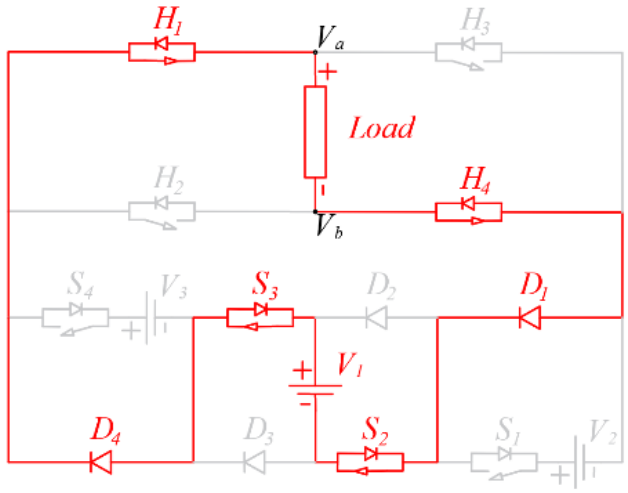


Figure 4.11 Mode 1 (+) - generation of $+1V_{dc}$ output voltage

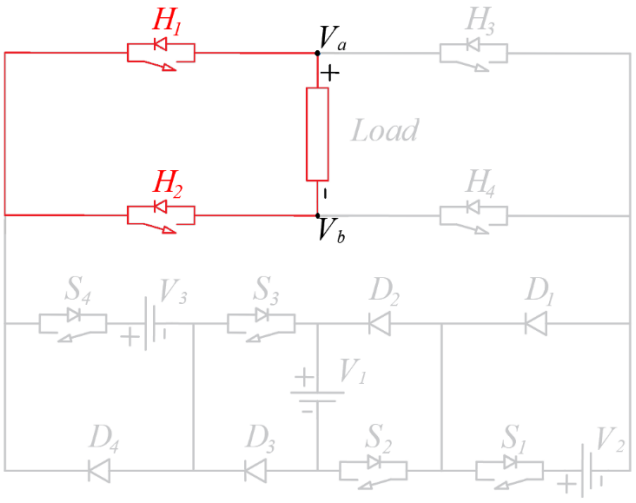


Figure 4.12 Mode 0 (I) - generation of $0V_{dc}$ output voltage

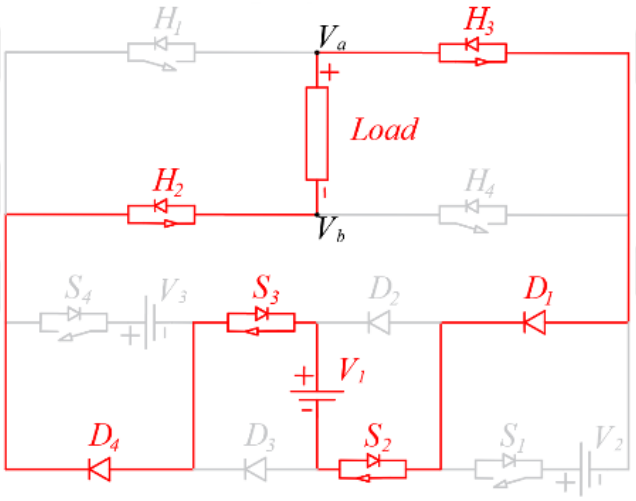


Figure 4.13 Mode 1 (-) - generation of $-1V_{dc}$ output voltage

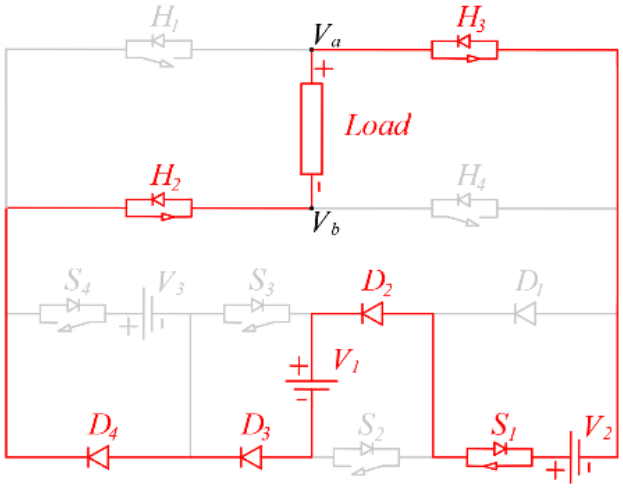


Figure 4.14 Mode 2 (-) - generation of $-2V_{dc}$ output voltage

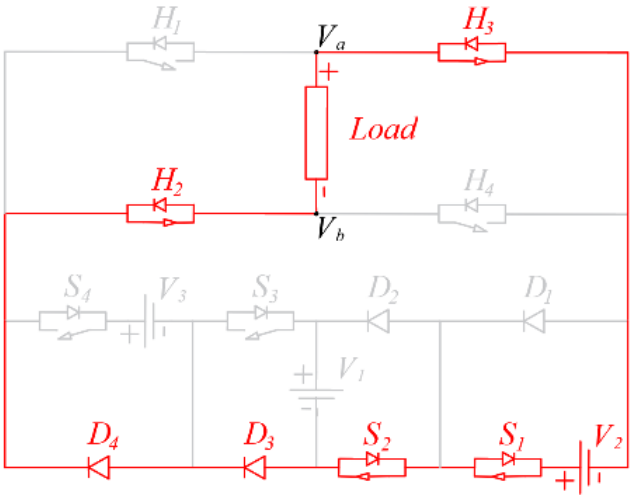


Figure 4.15 Mode 3 (-) - generation of -3V_{dc} output voltage

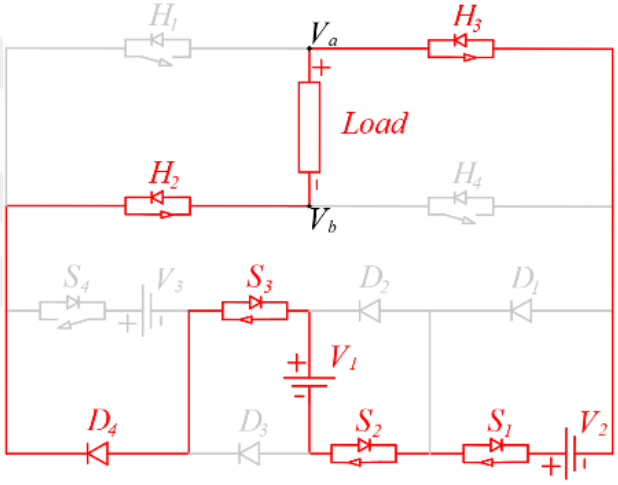


Figure 4.16 Mode 4 (-) - generation of -4V_{dc} output voltage

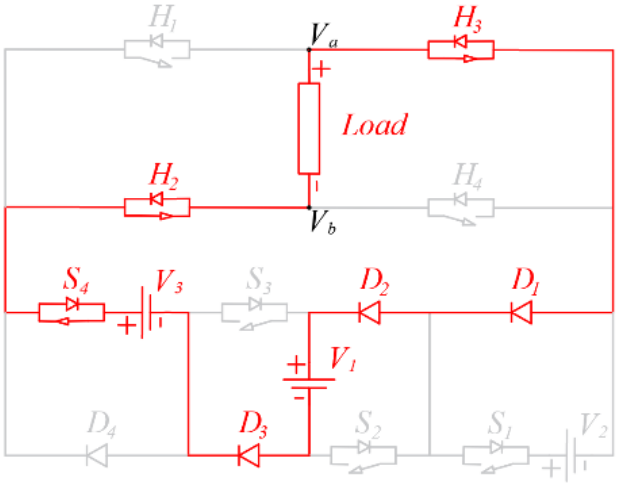


Figure 4.17 Mode 5 (-) - generation of -5V_{dc} output voltage

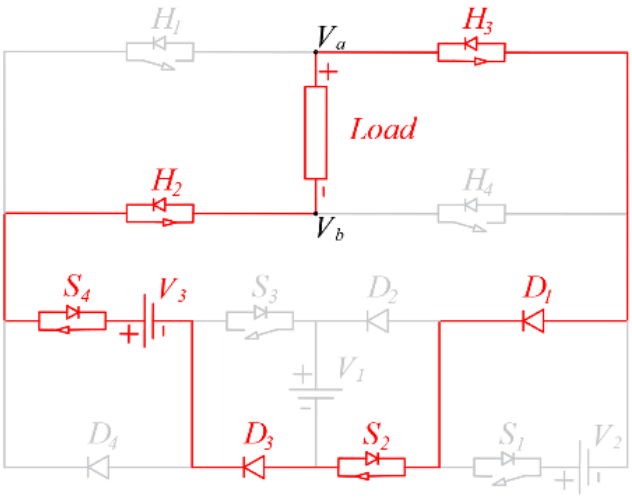


Figure 4.18 Mode 6 (-) - generation of -6V_{dc} output voltage

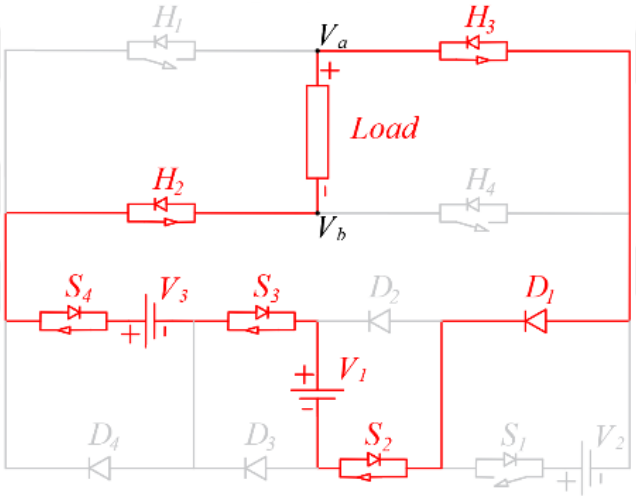


Figure 4.19 Mode 7 (-) - generation of -7V_{dc} output voltage

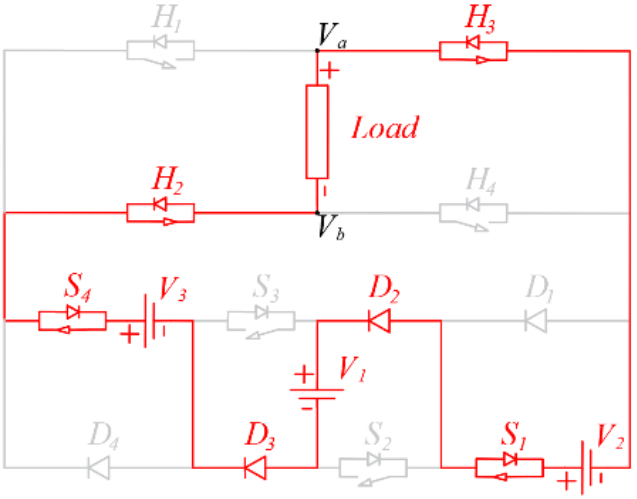


Figure 4.20 Mode 8 (-) - generation of -8V_{dc} output voltage

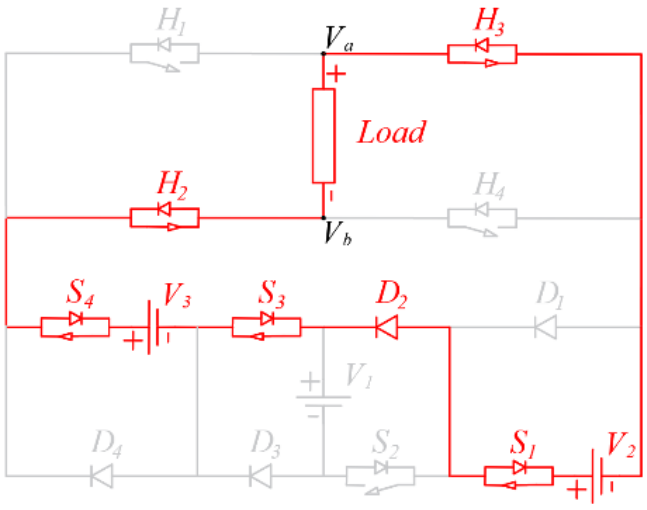


Figure 4.21 Mode 9 (-) - generation of -9V_{dc} output voltage

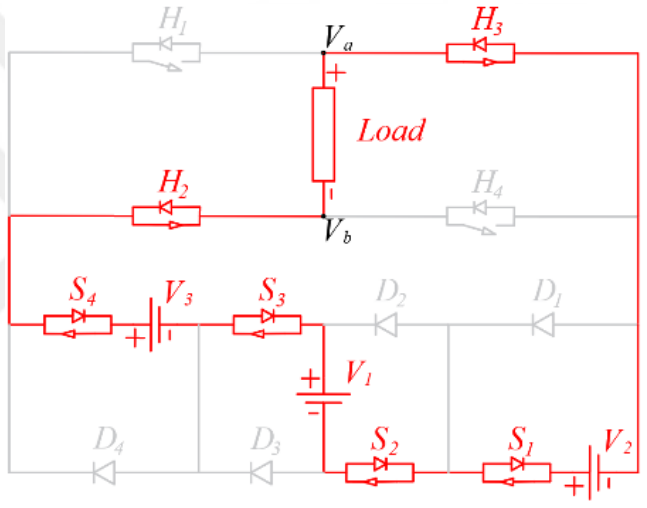


Figure 4.22 Mode 10 (-) - generation of -10V_{dc} output voltage

In the operation of a twenty-one-level MLI, each distinct output voltage level is achieved through a specific combination of conducting switches and source configurations that dictate the current flow path through the inverter circuitry. These combinations are organized into discrete operating modes based on the polarity and magnitude of the output voltage, with Modes 1(+) through 10(+) representing positive voltage levels and Modes 1(-) through 10(-) representing their negative counterparts. Each mode uses a specific configuration of switches, diodes, and sources to direct the load current and establish the resulting DC output voltage.

In Mode 10 (+), switches S_1, S_2, S_3, S_4, H_1 and H_4 are conducting. The load current flows through the path $V_2 \rightarrow S_1 \rightarrow S_2 \rightarrow V_1 \rightarrow S_3 \rightarrow V_3 \rightarrow S_4 \rightarrow H_1 \rightarrow L \rightarrow H_4 \rightarrow$

V_2, with all three sources ($V_2 + V_1 + V_3$) supplying the circuit, producing an output of $+10V_{dc}$.

In Mode 9 (+), switches S_1, S_3, S_4, D_2, H_1 and H_4 are conducting, and the load current flows through $V_2 \rightarrow S_1 \rightarrow D_2 \rightarrow S_3 \rightarrow V_3 \rightarrow S_4 \rightarrow H_1 \rightarrow L \rightarrow H_4 \rightarrow V_2$. Sources ($V_2 + V_3$) supply the circuit, resulting in $+9V_{dc}$.

In Mode 8 (+), switches S_1, S_4, D_2, D_3, S_4, H_1 and H_4 are conducting, with the load current path $V_2 \rightarrow S_1 \rightarrow D_2 \rightarrow V_1 \rightarrow D_3 \rightarrow V_3 \rightarrow S_4 \rightarrow H_1 \rightarrow L \rightarrow H_4 \rightarrow V_2$. The sources ($V_2 + V_3 - V_1$) supply the circuit, producing $+8V_{dc}$.

In Mode 7 (+), switches D_1, S_2, S_3, S_4, H_1 and H_4 are conducting, and the current flows through $D_1 \rightarrow S_2 \rightarrow V_1 \rightarrow S_3 \rightarrow V_3 \rightarrow S_4 \rightarrow H_1 \rightarrow L \rightarrow H_4 \rightarrow D_1$. The sources ($V_1 + V_3$) supply the circuit, producing $+7V_{dc}$.

In Mode 6 (+), switches D_1, S_2, D_3, S_4, H_1 and H_4 are conducting, with the load current path $D_1 \rightarrow S_2 \rightarrow D_3 \rightarrow V_3 \rightarrow S_4 \rightarrow H_1 \rightarrow L \rightarrow H_4 \rightarrow D_1$. Here, only V_3 supplies the circuit, producing $+6V_{dc}$.

In Mode 5 (+), switches D_1, D_2, D_3, S_4, H_1 and H_4 are conducting, and the current flows through $D_1 \rightarrow D_2 \rightarrow V_1 \rightarrow D_3 \rightarrow V_3 \rightarrow S_4 \rightarrow H_1 \rightarrow L \rightarrow H_4 \rightarrow D_1$. The sources ($V_3 - V_1$) supply the circuit, resulting in $+5V_{dc}$.

In Mode 4 (+), switches S_1, S_2, S_3, D_4, H_1 and H_4 are conducting, and the load current flows through $V_2 \rightarrow S_1 \rightarrow S_2 \rightarrow V_1 \rightarrow S_3 \rightarrow D_4 \rightarrow H_1 \rightarrow L \rightarrow H_4 \rightarrow V_2$. The sources ($V_1 + V_2$) supply the circuit, producing $+4V_{dc}$.

In Mode 3 (+), switches S_1, S_2, D_3, D_4, H_1 and H_4 are conducting, and the current flows through $V_2 \rightarrow S_1 \rightarrow S_2 \rightarrow D_3 \rightarrow D_4 \rightarrow H_1 \rightarrow L \rightarrow H_4 \rightarrow D_1$. Here, only V_2 supplies the circuit, producing $+3V_{dc}$.

In Mode 2 (+), switches S_1, D_2, D_3, D_4, H_1 and H_4 are conducting, with the load current path $V_2 \rightarrow S_1 \rightarrow D_2 \rightarrow V_1 \rightarrow D_3 \rightarrow D_4 \rightarrow H_1 \rightarrow L \rightarrow H_4 \rightarrow V_2$. The sources ($V_2 - V_1$) supply the circuit, producing $+2V_{dc}$.

In Mode 1 (+), switches D_1, S_2, S_3, D_4, H_1 and H_4 are conducting, and the load current flows through $D_1 \rightarrow S_2 \rightarrow V_1 \rightarrow S_3 \rightarrow D_4 \rightarrow H_1 \rightarrow L \rightarrow H_4 \rightarrow D_1$. Here, only V_1 supplies the circuit, producing $+1V_{dc}$.

For the negative modes, in Mode 1 (-), switches D_1, S_2, S_3, D_4, H_2 and H_3 are conducting, and the load current flows through $D_1 \rightarrow S_2 \rightarrow V_1 \rightarrow S_3 \rightarrow D_4 \rightarrow H_2 \rightarrow L \rightarrow H_3 \rightarrow D_1$. Here, only V_1 supplies the circuit, producing $-1V_{dc}$.

In Mode 2 (-), switches S_1, D_2, D_3, D_4, H_2 and H_3 are conducting, with the load current path $V_2 \rightarrow S_1 \rightarrow D_2 \rightarrow V_1 \rightarrow D_3 \rightarrow D_4 \rightarrow H_2 \rightarrow L \rightarrow H_3 \rightarrow V_2$. The sources ($V_2$ - V_1) supply the circuit, producing $-2V_{dc}$.

In Mode 3 (-), switches S_1, S_2, D_3, D_4, H_2 and H_3 are conducting, and the current flows through $V_2 \rightarrow S_1 \rightarrow S_2 \rightarrow D_3 \rightarrow D_4 \rightarrow H_2 \rightarrow L \rightarrow H_3 \rightarrow D_1$. Here, only V_2 supplies the circuit, producing $-3V_{dc}$.

In Mode 4 (-), switches S_1, S_2, S3, D_4, H_2 and H_3 are conducting, and the load current flows through $V_2 \rightarrow S_1 \rightarrow S_2 \rightarrow V_1 \rightarrow S_3 \rightarrow D_4 \rightarrow H_2 \rightarrow L \rightarrow H_3 \rightarrow V_2$. The sources ($V_1$ + V_2) supply the circuit, producing $-4V_{dc}$.

In Mode 5 (-), switches D_1, D_2, D_3, S_4, H_2 and H_3 are conducting, and the current flows through $D_1 \rightarrow D_2 \rightarrow V_1 \rightarrow D_3 \rightarrow V_3 \rightarrow S_4 \rightarrow H_2 \rightarrow L \rightarrow H_3 \rightarrow D_1$. The sources ($V_3$ - V_1) supply the circuit, resulting in $-5V_{dc}$.

In Mode 6 (-), switches D_1, S_2, D_3, S_4, H_2 and H_3 are conducting, with the load current path $D_1 \rightarrow S_2 \rightarrow D_3 \rightarrow V_3 \rightarrow S_4 \rightarrow H_2 \rightarrow L \rightarrow H_3 \rightarrow D_1$. Here, only V_3 supplies the circuit, producing $-6V_{dc}$.

In Mode 7 (-), switches D_1, S_2, S_3, S_4, H_2 and H_3 are conducting, and the current flows through $D_1 \rightarrow S_2 \rightarrow V_1 \rightarrow S_3 \rightarrow V_3 \rightarrow S_4 \rightarrow H_2 \rightarrow L \rightarrow H_3 \rightarrow D_1$. The sources ($V_1$ + V_3) supply the circuit, producing $-7V_{dc}$.

In Mode 8 (-), switches S_1, S_4, D_2, D_3, S_4, H_2 and H_3 are conducting, with the load current path $V_2 \rightarrow S_1 \rightarrow D_2 \rightarrow V_1 \rightarrow D_3 \rightarrow V_3 \rightarrow S_4 \rightarrow H_2 \rightarrow L \rightarrow H_3 \rightarrow V_2$. The sources ($V_2$ + V_3 - V_1) supply the circuit, producing $-8V_{dc}$.

In Mode 9 (-), switches S_1, S_3, S_4, D_2, H_2 and H_3 are conducting, and the load current flows through $V_2 \rightarrow S_1 \rightarrow D_2 \rightarrow S_3 \rightarrow V_3 \rightarrow S_4 \rightarrow H_2 \rightarrow L \rightarrow H_3 \rightarrow V_2$. Sources ($V_2$ + V_3) supply the circuit, resulting in $-9V_{dc}$.

Finally, in Mode 10 (-), switches S_1, S_2, S_3, S_4, H_2 and H_3 are conducting. The load current flows through the path $V_2 \rightarrow S_1 \rightarrow S_2 \rightarrow V_1 \rightarrow S_3 \rightarrow V_3 \rightarrow S_4 \rightarrow H_2 \rightarrow L \rightarrow H_3 \rightarrow V_2$, with all three sources (V_2 + V_1 + V_3) supplying the circuit, producing an output of $-10V_{dc}$.

Figures 4.6 through figure 4.26 illustrate the current conduction paths and the associated configurations for each mode in detail. These mode-wise diagrams visually represent the internal operation of the inverter across all twenty-one output voltage levels, supporting the textual descriptions provided. In each figure, the direction of current, the contributing voltage sources (V_1, V_2, V_3), and the active switching elements are clearly indicated to enhance comprehension of the switching logic.

5
SIMULATION MODELING AND PERFORMANCE PARAMETERS

This chapter presents the simulation-based evaluation framework developed to validate the performance of the proposed asymmetric twenty-one level inverter topology. Simulation modeling plays a crucial role in power electronics research, as it enables the prediction of system behavior under various operational scenarios before physical prototyping. In this context, a comprehensive simulation environment is established to test the converter's performance across a range of load conditions, with realistic design assumptions and system parameters.

The chapter begins by describing the simulation environment, including the modeling tools, time step configurations, and fundamental assumptions employed. Next, the considered load types-resistive, inductive, and dynamic-are introduced, along with their electrical characteristics. Following this, critical performance metrics such as THD, Maximum Blocking Voltage (MBV), and TSV are defined and calculated to assess waveform quality, component stress, and operational efficiency. Additional indices such as Normalized Voltage Stress (NVS), CF, and Component Level Factor (F_{ccl}) are also evaluated to provide a holistic view of the inverter's effectiveness. The final section provides a detailed analysis of power losses, offering insights into the thermal and energy efficiency behavior of the system.

5.1 Simulation Environment and Assumptions

The reliability and accuracy of simulation studies depend significantly on how well the chosen simulation environment and underlying assumptions represent real-world system behavior. In this context, PSIM software has been utilized to analyze the performance of the proposed 21-level MLI topology. The simulation environment is configured based on ideal assumptions, where circuit parameters are considered lossless, control algorithms operate under ideal conditions, and switching components are free from parasitic effects such as switching losses and voltage drops. This modeling approach establishes a suitable framework to evaluate

the theoretical performance limits of the proposed topology and to validate the accuracy of the implemented control strategy.

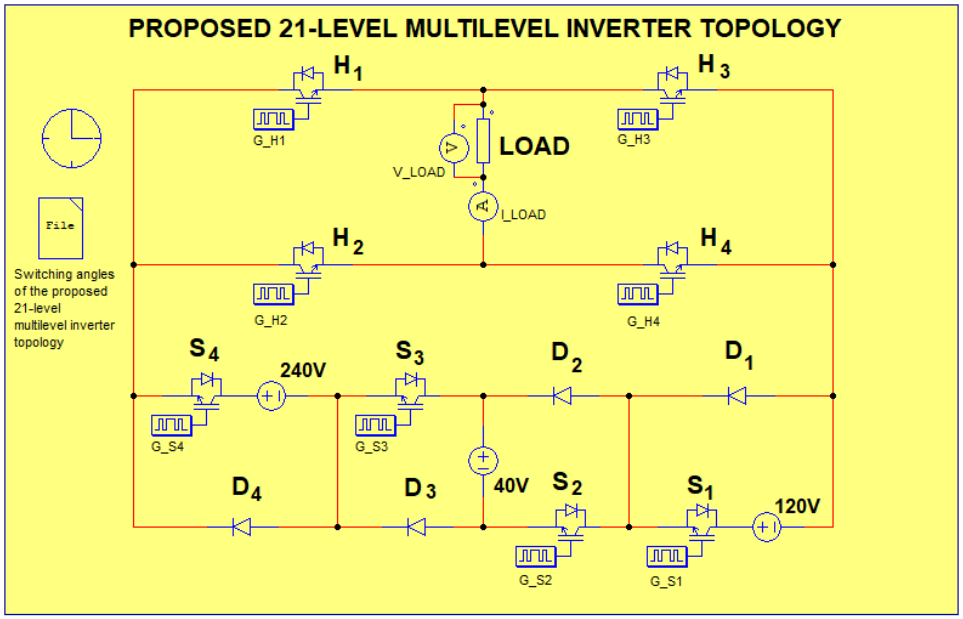


Figure 5.1 PSIM simulation of the proposed 21-level MLI topology

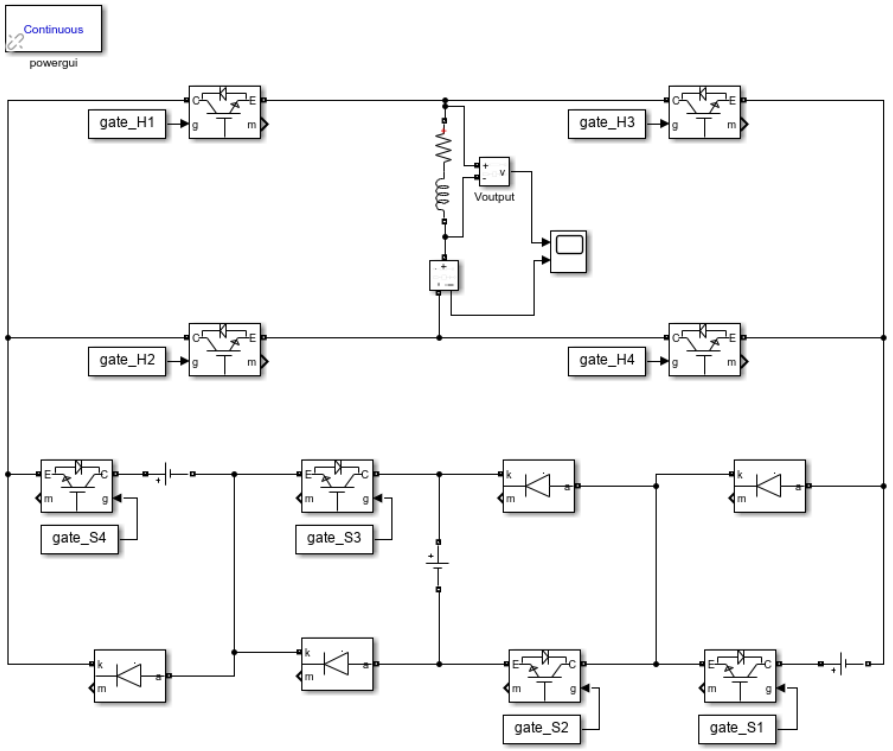


Figure 5.2 MATLAB/Simulink simulation of the proposed 21-level MLI topology

In the simulation process, different methods were adopted to apply the gating signals that drive the proposed inverter topology within the PSIM and MATLAB/Simulink environments, as shown in Figure 5.1 and Figure 5.2, respectively. In the PSIM platform, the switching signals were generated by calculating the exact switching angles required by the NLC strategy. These angles were then assigned to each gating block using the built-in "File Control" feature in PSIM. The gating blocks were configured to apply the corresponding switching instants by referencing these preloaded angles, allowing accurate control over the inverter's switching events and output waveform synthesis.

In contrast, the MATLAB/Simulink simulation environment used externally stored gate signal data, which had been previously exported in Comma-Separated Values format. These Comma-Separated Values files contained time-aligned switching data for each gate. A pre-processing routine was executed in MATLAB to read these datasets, convert them into time-series format, and assign them to the base workspace. These time-series objects were then linked to the Simulink circuit model to drive the switching elements. This approach ensured synchronization between the gate signals and simulation time, allowing precise control of switching behaviour during simulations.

The circuit consists of cascaded submodules and switching components arranged to generate stepped voltage levels at the output. Each switching device is configured in accordance with the control strategy to ensure accurate level generation and optimized performance. This simulation model serves as the foundation for evaluating the inverter’s steady-state and dynamic behavior under various loading conditions in the subsequent analyses.

This section provides an in-depth description of the simulation parameters and operational assumptions used to evaluate the performance of the proposed twenty-one-level MLI topology. The simulations were conducted using established digital platforms to analyze the system’s ability to produce high-fidelity output voltage waveforms, validate the accuracy of the NLC switching strategy, and observe the inverter’s dynamic behavior under predefined conditions. All simulation parameters were carefully chosen to mirror realistic operating scenarios, thereby increasing the relevance of the results for practical implementation and supporting the feasibility of future hardware-based applications.

The performance of the proposed twenty-one-level MLI topology was thoroughly evaluated through independent simulations conducted in both PSIM environments. These platforms were employed to analyze various system characteristics, including switching behavior, output waveform quality, and transient responses. The switching frequency of the proposed inverter topology is set to 50 Hz. This low-frequency operation significantly reduces switching losses and mitigates the need for bulky filtering components, thereby enhancing overall system efficiency. The required switching signals were generated using the NLC modulation strategy, which ensures the generation of high-quality stepped output voltages even at low switching frequencies.

To achieve the twenty-one-level stepped voltage waveform, three independent and asymmetrical DC voltage sources with magnitudes of V_1 = 40 V, V_2 = 120 V, and V_3 = 240 V were employed. The asymmetrical configuration allows the inverter to generate a higher number of output levels using fewer switching devices compared to symmetric counterparts. This contributes to reduced circuit complexity and lower THD in the output waveform.

In conclusion, the simulation environment and assumptions provide a controlled platform for evaluating the fundamental performance characteristics of the proposed 21-level MLI topology under idealized conditions. For future studies, it is intended to incorporate non-idealities such as switching losses, voltage drops, and control algorithm delays to enhance the model's fidelity and bring it closer to real-world operation.

5.2 Load Configurations and Parameters

Initially, the system was tested under a purely R load of 100 Ω. This loading condition facilitated a clear and direct evaluation of the inverter’s steady-state output characteristics. Figure 5.3 presents the output voltage waveform of the proposed topology under an R load. It illustrates the successful generation of distinct and evenly spaced voltage levels, with smooth transitions confirming the system’s effective stepped voltage synthesis.

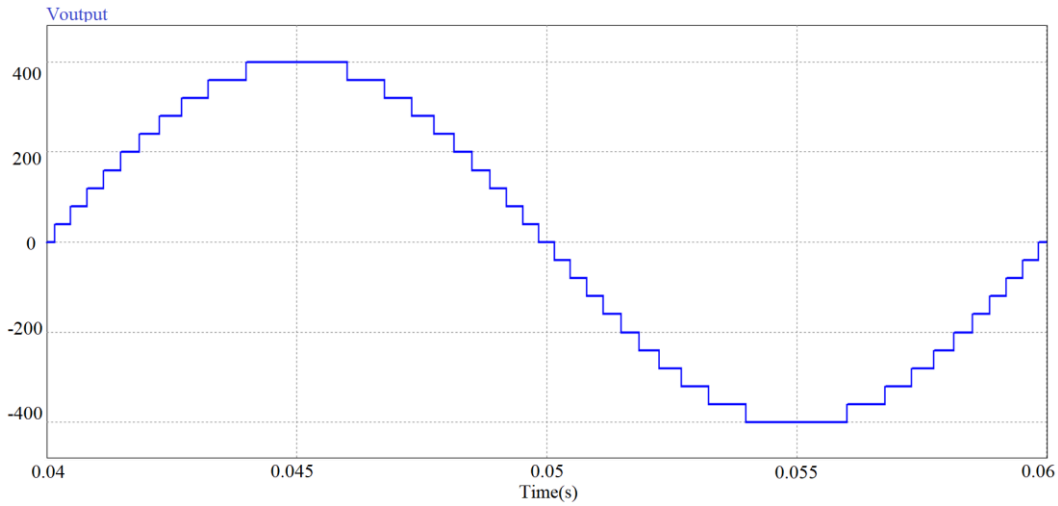


Figure 5.1 Output voltage waveform of the proposed 21-level MLI topology under R load

As illustrated in Figure 5.3, the output voltage waveform generated by the proposed 21-level inverter under a purely R load exhibits a clearly defined stepped structure, with the peak voltage reaching 400 V. The waveform demonstrates a close alignment with the reference sinusoidal signal, thereby validating the accuracy and effectiveness of the NLC technique in producing finely regulated voltage levels across the output.

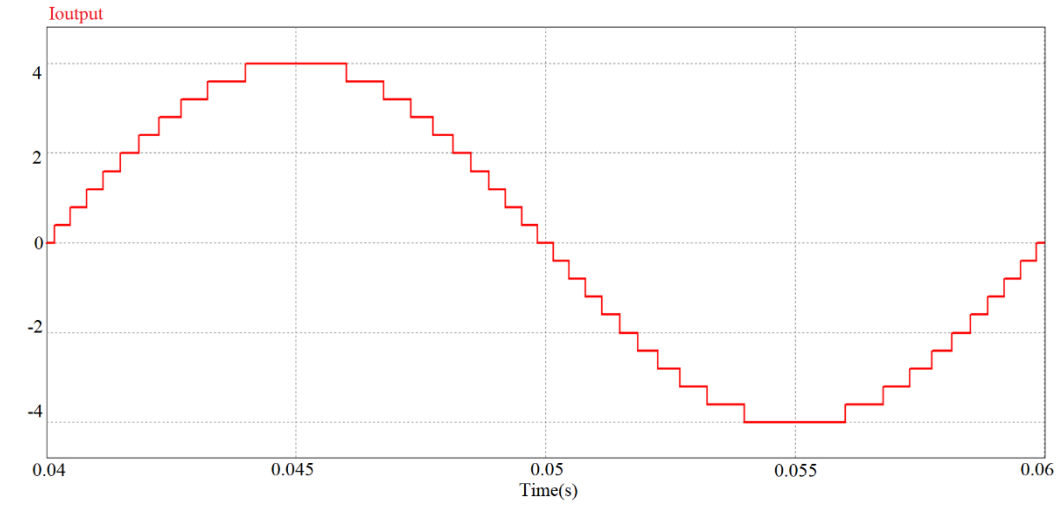


Figure 5.2 Output current waveforms of the proposed 21-level MLI topology under R load

Figure 5.4 presents the output current waveforms of the proposed 21-level MLI topology when operating under a purely R load. The voltage waveform exhibits a near-sinusoidal profile with clearly defined levels, validating the proper functioning of the level generation mechanism. The corresponding output current under R

loading is illustrated in the same figure. For a R load of 100 Ω, the peak current reaches approximately 4 A. The current waveform remains sinusoidal and in phase with the voltage, demonstrating the clean, stable, and distortion-free operation of the inverter under linear load conditions.

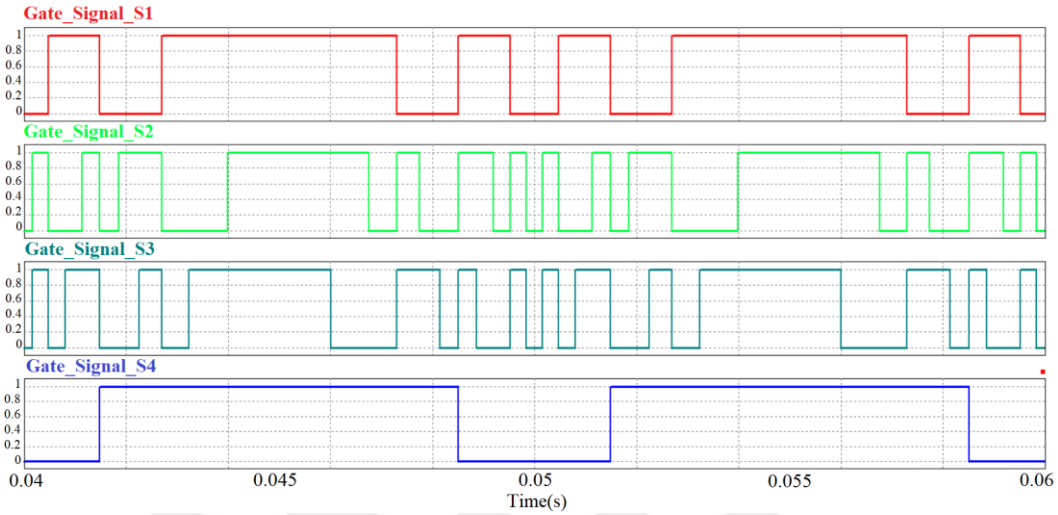


Figure 5.3 Switching signals of switches S_1-S_4 in the proposed 21-level MLI topology

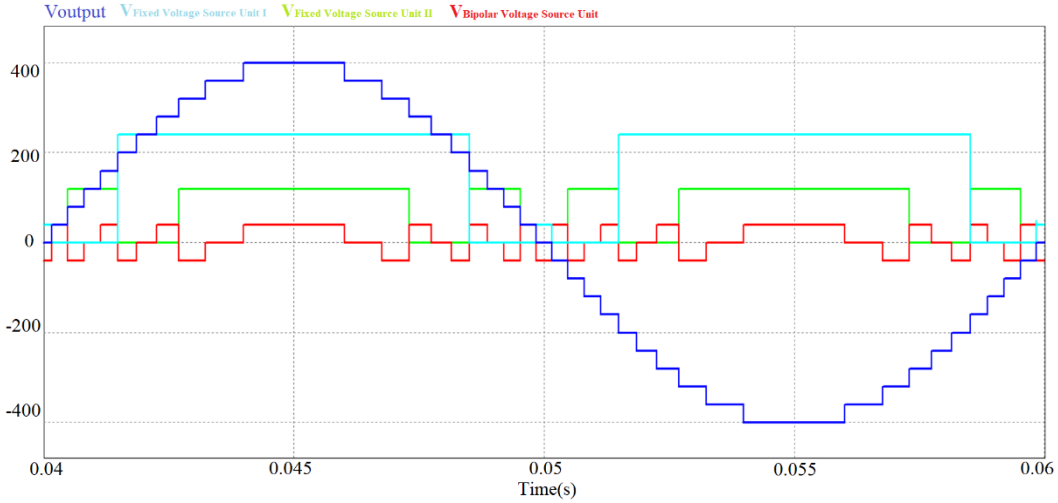


Figure 5.4 Voltage waveforms of FVSU I, FVSU II, BVSU, and the output waveform as the sum of all voltage units

In addition to the output voltage and current waveforms, Figure 5.5 illustrates the switching behavior of the proposed inverter. This figure presents a detailed representation of the gate signals generated through the NLC technique. The switching pulses demonstrate well-synchronized and accurately timed transitions, which are essential for generating the correct voltage levels at the output. These

results confirm the proper functionality of the switching devices and highlight the effectiveness of the NLC method in reducing switching losses.

Figure 5.6 illustrates the individual voltage waveforms generated by FVSU I, FVSU II, and the BVSU within the proposed MLI topology. The output waveform, shown as the bottom trace, is obtained by the stepwise summation of all three voltage source units. This composition results in a high-resolution staircase voltage waveform, which is critical for reducing THD and improving output waveform quality.

Figure 5.7 illustrates the Fast Fourier Transform (FFT) analysis of the output voltage waveform obtained from the proposed twenty-one-level inverter topology under a purely R load. The spectral distribution reveals the fundamental frequency component and associated harmonic orders. The THD is calculated as 3.90%, indicating effective harmonic suppression and high-quality output voltage.

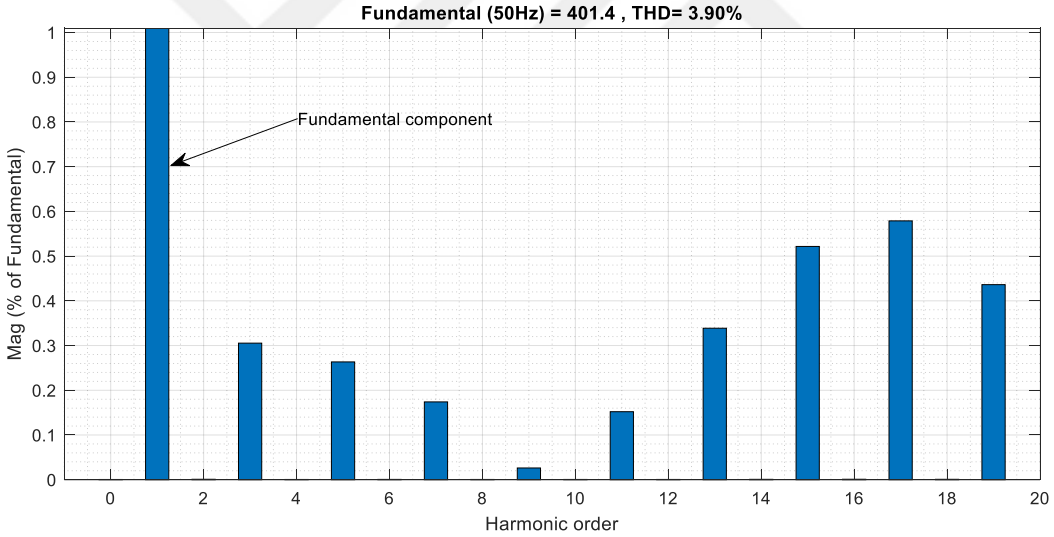


Figure 5.5 FFT analysis of the proposed twenty-one level output voltage waveform under R load

Figures 5.8 and 5.9 present the output voltage and current waveforms of the proposed 21-level MLI topology unde a RL load composed of a 100 Ω resistor and a 10 mH inductor, utilizing NLC as the modulation technique.

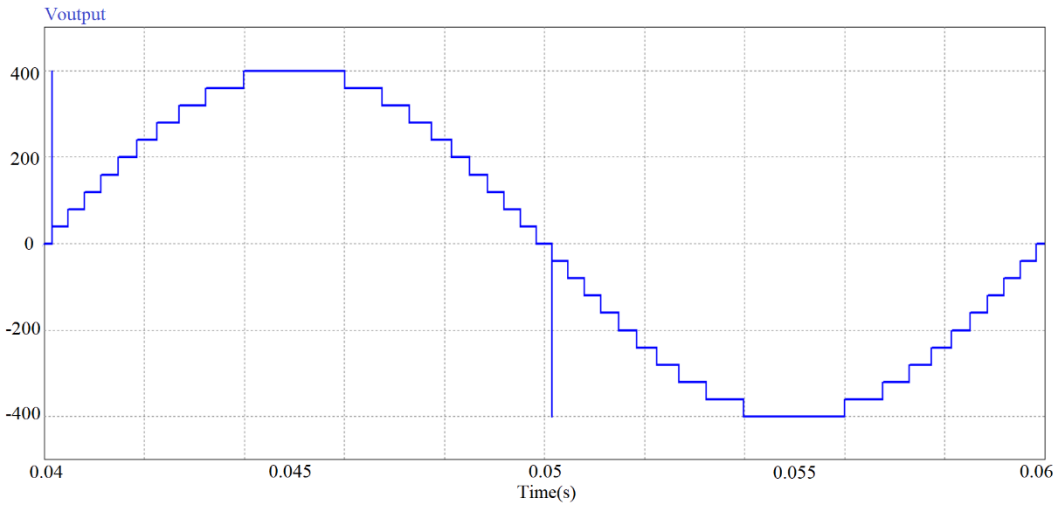


Figure 5.6 Output voltage waveform of the proposed 21-level MLI topology under RL load

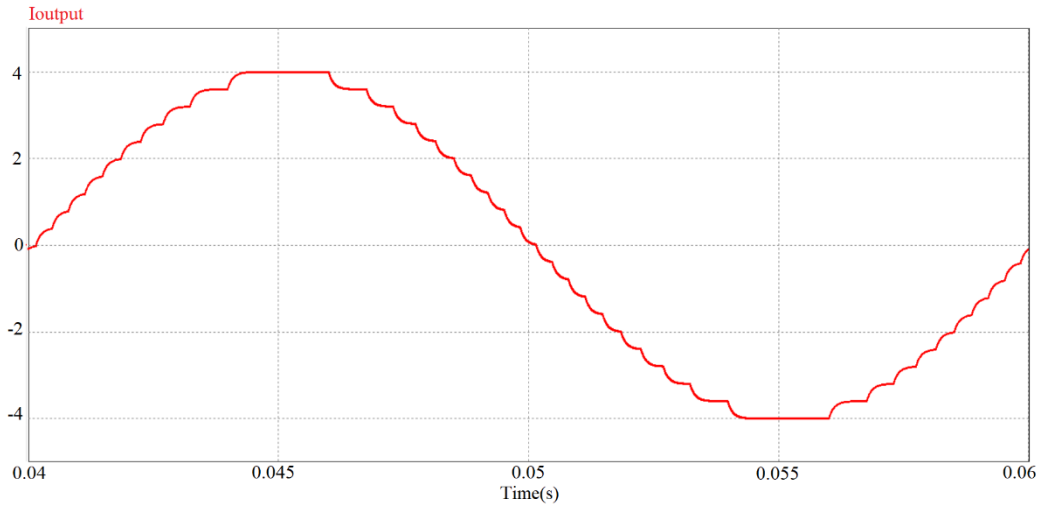


Figure 5.7 Output current waveform of the proposed 21-level MLI topology under RL load

In Figure 5.8, the output voltage waveform of the inverter is shown. As observed, the NLC technique selects the voltage level closest to the reference signal, resulting in a step-like waveform that characterizes the 21-level structure. The waveform reflects the distinct voltage steps achieved by the inverter.

Figure 5.9 illustrates the corresponding output current under the same load conditions. Due to the inductive nature of the load, the current waveform exhibits smoother transitions compared to the stepped voltage waveform. This demonstrates that the proposed MLI topology, combined with NLC modulation, operates stably and effectively under RL loading conditions.

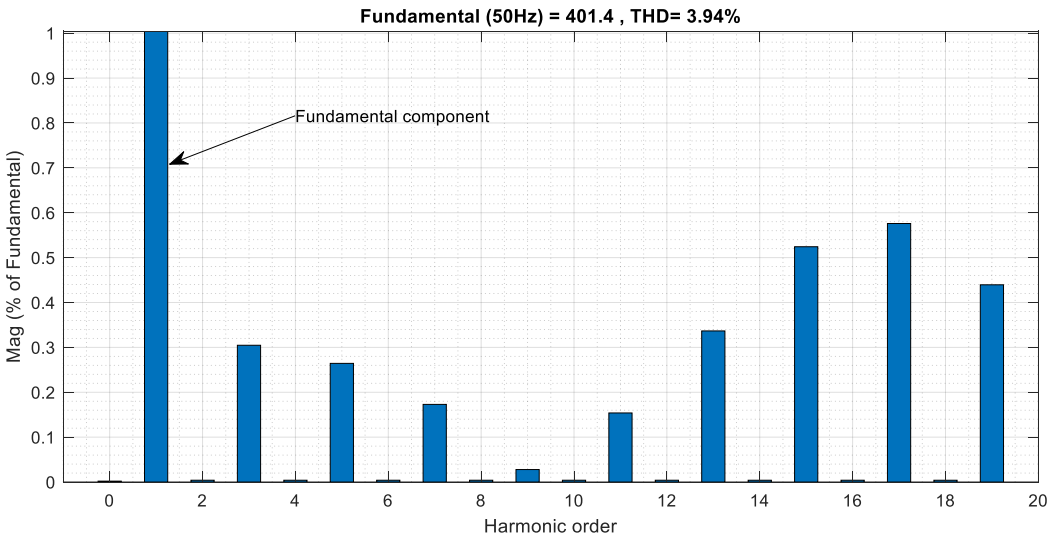


Figure 5.8 FFT analysis of the proposed twenty-one level output voltage waveform under RL load

Figure 5.10 presents the FFT analysis of the output voltage waveform generated by the proposed twenty-one-level MLI under an RL load condition without the implementation of any snubber circuits. The spectral distribution reveals the dominance of the fundamental frequency component, while the presence of higher-order harmonics-particularly around the 15th and 17th orders-is noticeable. Despite being within allowable bounds, the THD of 3.94% shows the impact of parasitic inductances and switching transients under RL loads. This result emphasizes how important it is to put in place suitable snubber networks to further reduce harmonic content and enhance the quality of the output waveform.

The analysis of output waveforms and switching signals verifies the reliable performance of the proposed 21-level MLI topology under R and RL load conditions. These results confirm the correct implementation of the NLC modulation strategy and the precise operation of the power switches. Based on these validated observations, the following section introduces the design methodology and parameter determination for the snubber circuits implemented in the proposed inverter topology.

5.3 Snubber Circuit Design and Parameter Evaluation

Snubber circuits safeguard semiconductor switching devices from over voltages, abrupt current transients, and EMI, ensuring safe and steady switching in power electronic systems. The effectiveness and performance of the entire converter

topology are directly impacted by the appropriate design of these circuits. The topologies of three basic snubber circuit types (turn-on, turn-off, and overvoltage snubbers) are examined in this section.

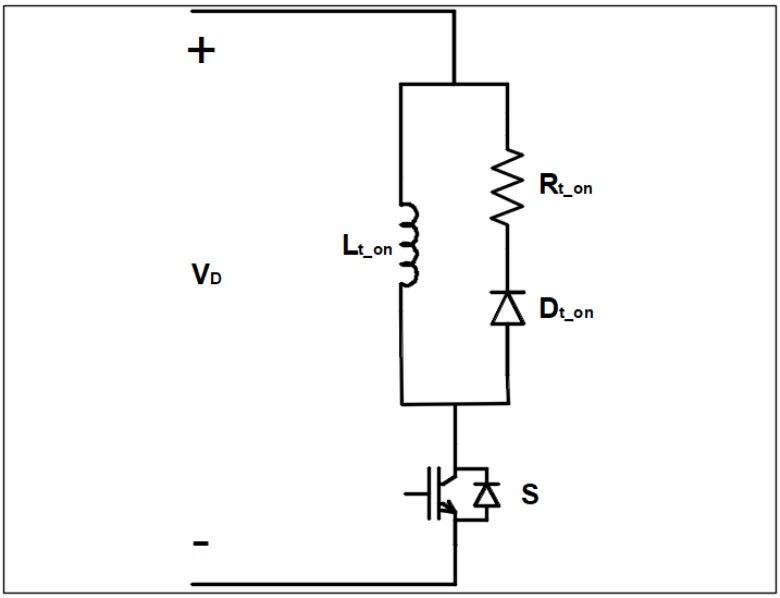


Figure 5.1 Turn-on snubber topology

Turn-on Snubbers are used to reduce excessive current spikes that happen during the conduction phase across switching devices. Because they lower turn-on losses, these snubber circuits are especially useful in applications requiring high switching frequencies. A resistor-diode network connected in reverse-parallel across the inductor and a tiny inductor connected in series with the switching element make up a standard turn-on snubber. The energy stored in the inductor is released across the resistor via the diode channel when the switch is turned off. Figure 5.11 shows a schematic illustration of this setup.

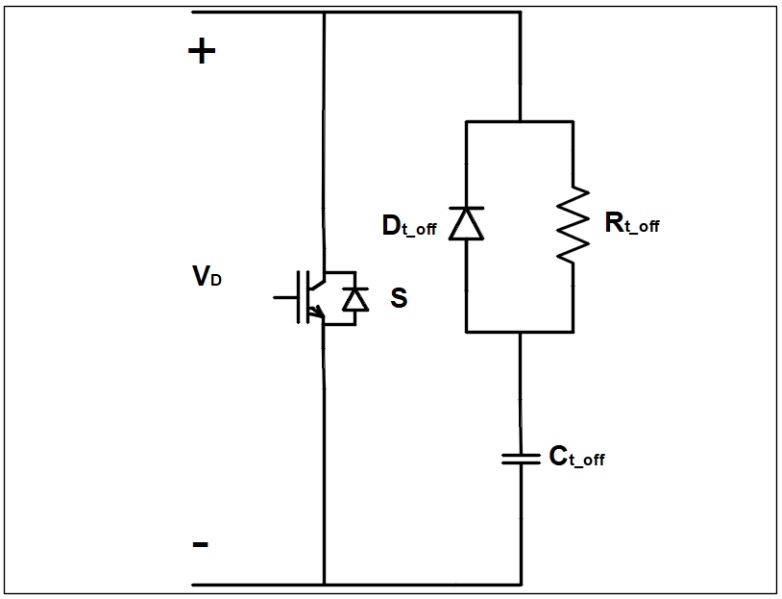


Figure 5.2 Turn-off snubber topology

This circuit is used to lessen problems that occur when switching devices are turned off. Its fundamental goal is to guarantee that until the current flowing through the device drops to zero, the voltage across the switching element stays zero or extremely low. Usually, a resistor and a decoupling capacitor are connected in series to form the circuit. A discharge safety diode is frequently connected in parallel with the resistor as well. The loop inductance is typically overlooked when determining the values of the resistor and capacitor because the circuit is mainly employed with purely R loads. Figure 5.12 displays this configuration's schematic depiction.

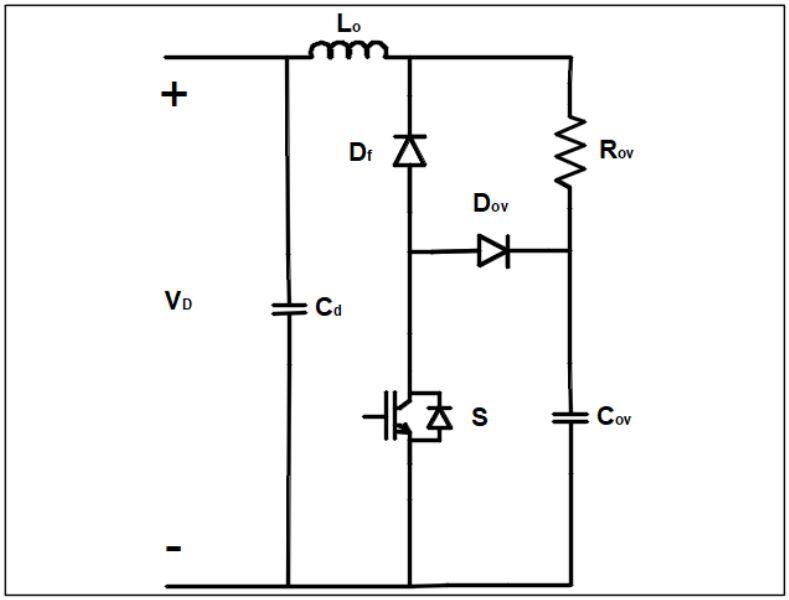


Figure 5.3 Overvoltage snubber topology

When the switching device turns off, a voltage overshoot across the load could happen if these parasitic inductances are taken into consideration. By using an overvoltage snubber circuit, this problem can be avoided. The circuit configuration is depicted in Figure 5.13.

In the proposed 21-level MLI topology, a turn-off snubber circuit is employed to suppress the voltage overshoot that occurs across the load during the turn-off period of the switching device. This circuit helps ensure that the voltage across the switch remains at a minimal level until the current falls to zero, thereby protecting the device from stress and improving overall reliability [127].

The equations provided in the figure represent the parameter calculations for the implemented turn-off snubber:

C_{t_off}: Turn-off snubber capacitor (5.1), responsible for absorbing and limiting transient energy.

R_{t_off}: Snubber resistor (5.2), used to dissipate the stored energy safely.

t_{fi}: Current fall time,

I_o: Peak current through the switch during operation,

V_d: DC link voltage.

Capacitor value is calculated as:

$$C_{t_off} = \frac{I_O . t_{fi}}{2.V_d} (5.1)$$

$$C_{t_off} = \frac{4 \times 0.7 \times 10^{-6}}{2 \times 400} = \frac{2.8 \times 10^{-6}}{800} = 3.5 \times 10^{-9} F = 3.5nF$$

Resistor value:

$$R_{t_off} > \frac{V_d}{0.2 \times I_O} (5.2)$$

$$R_{t_off} > \frac{400}{0.8} = 500\Omega$$

To ensure the capacitor is fully discharged before the next switching cycle, the minimum on-state time of the switch (5.3) must satisfy:

$$t_{on} > 2.3 \times R_s \times C_s (5.3)$$

$$t_{on} > 2.3 \times 500 \times 3.5 \times 10^{-9} = 4.025 \times 10^{-6} = 4.03us$$ [127]

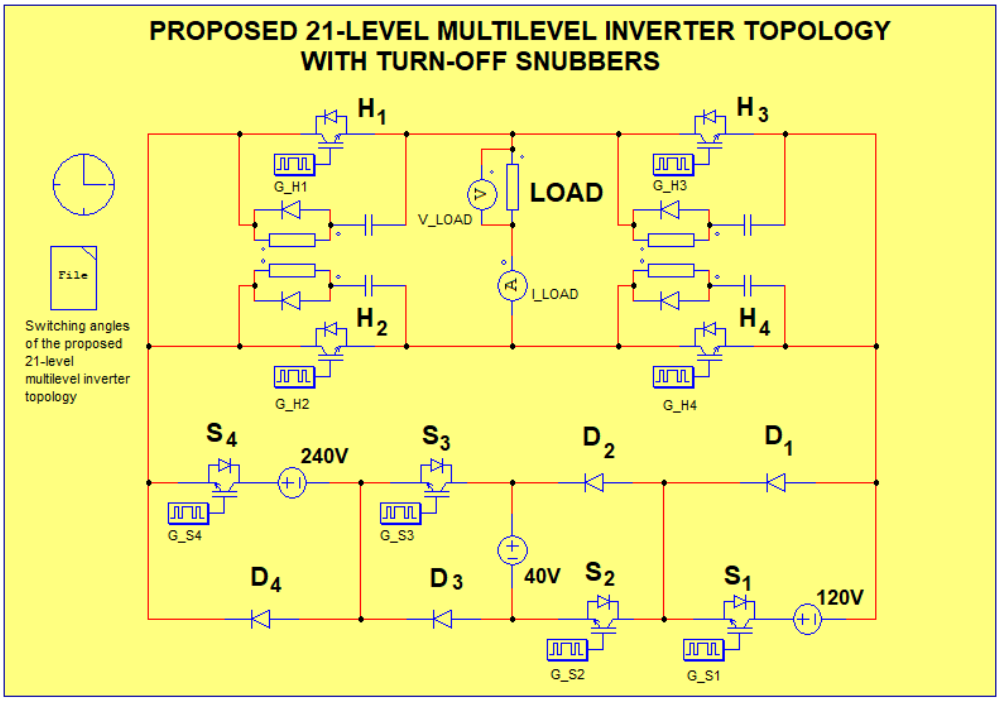


Figure 5.4 Proposed 21-Level MLI topology with turn-off snubber

In the proposed 21-level MLI topology, a turn-off snubber circuit is integrated to suppress voltage overshoots occurring during the switch turn-off event. The structural configuration and the placement of the turn-off snubber circuit are illustrated in detail in Figure 5.14. The calculated parameters were directly

implemented in the simulation model to evaluate the inverter's transient behaviour during the turn-off process. As a result, the effectiveness of the snubber design was verified by analysing the system's voltage-time and current-time characteristics under switching conditions.

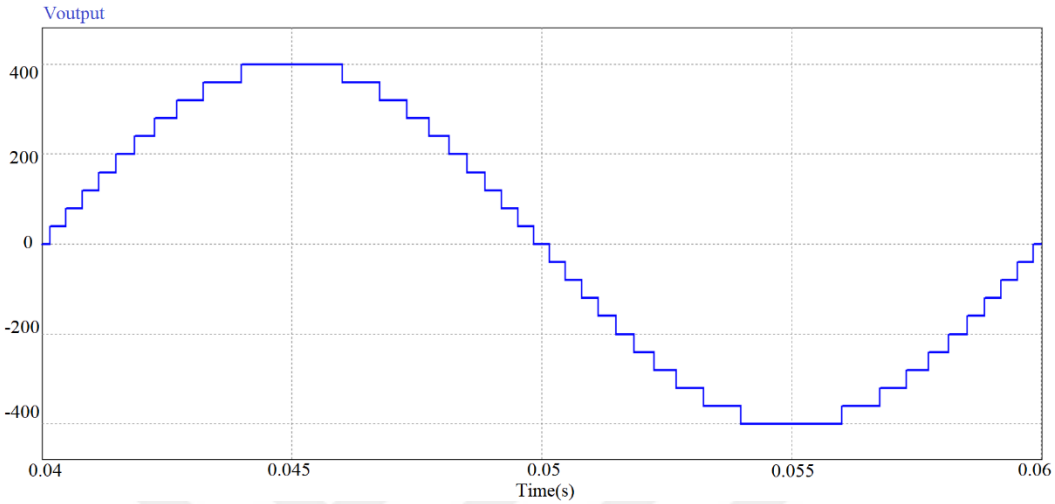


Figure 5.5 Output voltage waveform of the proposed 21-level MLI topology under RL load with turn-off snubber circuit

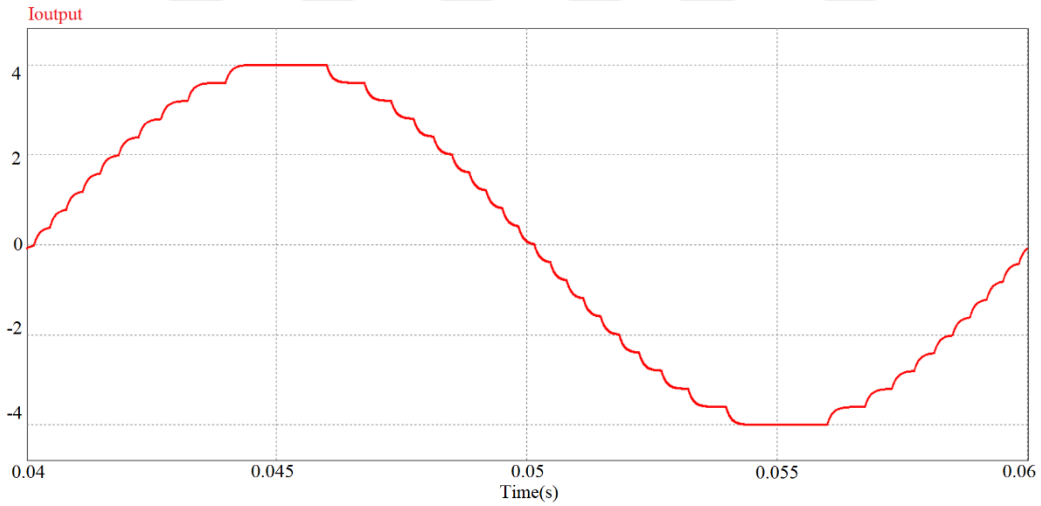


Figure 5.6 Output current waveform of the proposed 21-level MLI topology under RL load with turn-off snubber circuit

The output voltage and current behavior of the proposed 21-level MLI topology under RL load have been evaluated with the turn-off snubber circuit. As illustrated in Figure 5.15, the inclusion of the turn-off snubber effectively suppresses sharp voltage transitions and overshoots observed in the snubber less case. The abrupt steps and voltage spikes, clearly present without the snubber, are a result of uncontrolled energy feedback into the switching device.

Also, the current output waveform shown in Figure 5.16 exhibits a much smoother and more continuous profile when the overvoltage snubber is included. The mitigation of sharp transitions and saturation in the current curve particularly around zero-crossings indicates that the snubber significantly reduces EMI. These results confirm the positive influence of the turn-off snubber on both output voltage and output current characteristics of the inverter.

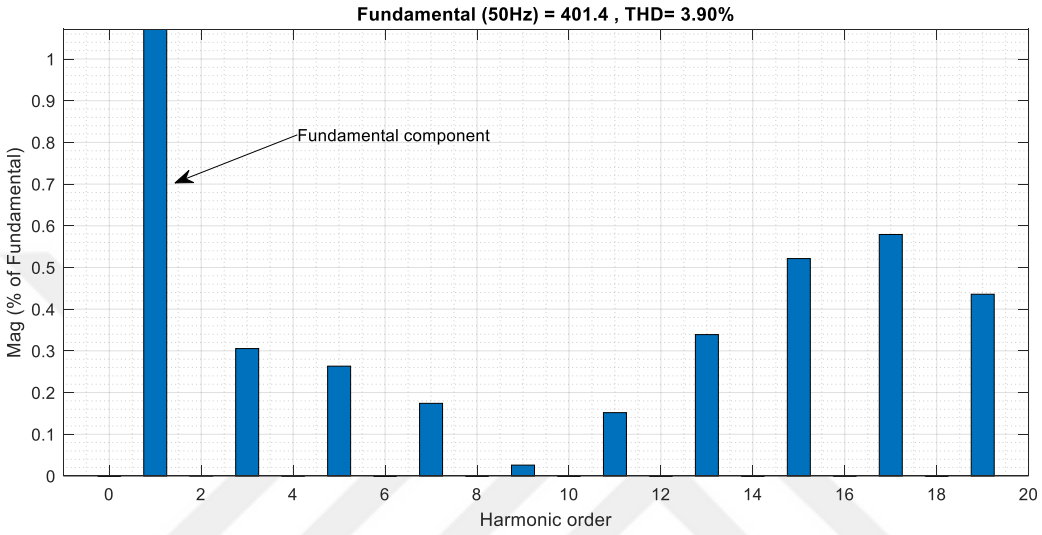


Figure 5.7 FFT analysis of the proposed twenty-one level output voltage waveform under RL load with turn-off snubber

Figure 5.17 presents the FFT analysis of the output voltage waveform for the proposed twenty-one-level MLI under an RL load. This analysis reflects the spectral behaviour after the integration of properly designed snubber circuits. While the fundamental component remains dominant, there is a notable reduction in the amplitude of higher-order harmonics. The THD value is observed to decrease compared to the case without snubber implementation. These results confirm that the snubber circuits effectively mitigate switching transients, suppress harmonic components, and enhance the overall output waveform quality.

5.4 Performance Metrics

Performance metrics play a pivotal role in the objective evaluation of MLI topologies by providing measurable criteria that reflect both technical efficiency and economic feasibility. These parameters enable detailed analysis of waveform fidelity, device voltage stress, circuit complexity, and cost-effectiveness, thereby guiding the selection and optimization of inverter designs. This section presents and

discusses a comprehensive set of key metrics, including THD for waveform quality, MBV, TSV, and Total Standing Voltage per unit (TSV_{pu}) for device voltage stress evaluation, NVS for comparative voltage loading, CF and Cost Function per Level (CF/L) for cost-performance analysis, and Component Level Factor for assessing structural complexity [128].

In the following subsections provide a detailed evaluation of the proposed 21-level MLI topology using the performance metrics previously discussed. Individual calculations and analyses are conducted for each parameter to assess the topology's technical capability, harmonic distortion performance, voltage stress levels across switching devices, cost-effectiveness, and structural complexity. The subsequent sections present the evaluation methodology, applied formulas, and quantitative results corresponding to each performance metric.

5.3.1 Total Harmonic Distortion

THD is a critical parameter for evaluating the quality of the output voltage waveform in MLIs. It quantifies the extent to which the output deviates from an ideal sinusoidal waveform due to the presence of harmonic components. Lower THD values are indicative of better waveform fidelity, reduced EMI, and improved power quality, which are essential in sensitive industrial and grid-connected applications. In MLIs, increasing the number of output levels generally results in a more sinusoidal waveform, thereby reducing THD. The proposed topology achieves a notable reduction in THD compared to conventional configurations, owing to its optimized switching strategy and effective voltage level synthesis [128].

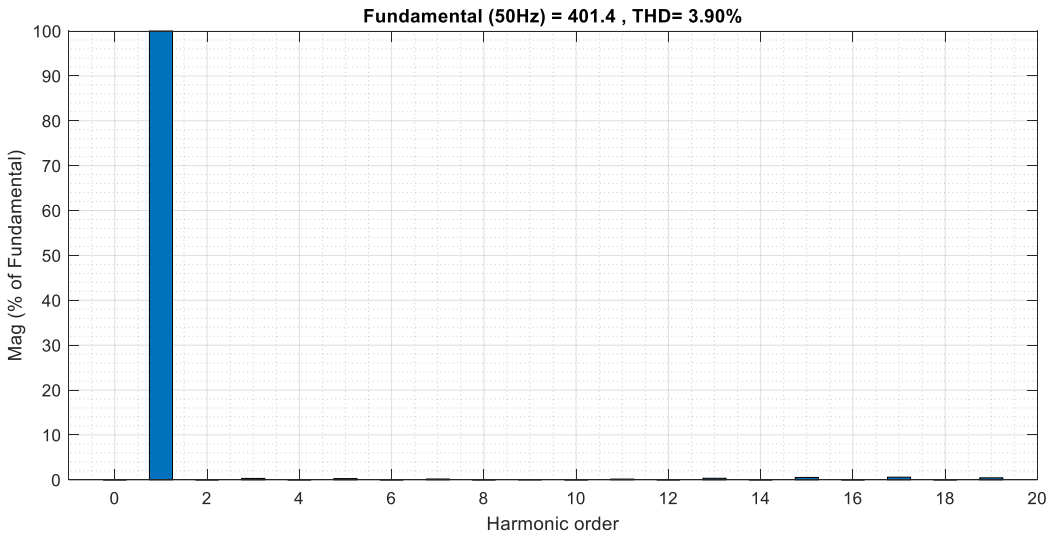


Figure 5.1 FFT spectrum of the output voltage of the proposed 21-level inverter with turn-off snubber under RL load

Furthermore, the spectral analysis shown in Figure 5.18 not only validates the suggested snubber-assisted inverter configuration's efficacy but also its viability. The amplitudes of higher-order harmonics are demonstrated to be negligibly small in relation to the fundamental component's magnitude, which serves as the 100% reference in the FFT analysis. This illustrates how well the turn-off snubber circuit suppresses harmonic distortion and transient voltage overshoots, producing an output waveform that closely matches an ideal sinusoid.

5.3.2 Maximum Blocking Voltage

MBV denotes the highest voltage level that a switch must withstand in the off state. This parameter plays a decisive role in the selection of semiconductor devices and directly impacts the insulation design, switching speed, and system cost. Topologies with lower MBV are generally preferred due to reduced stress and enhanced device longevity.

Figure 5.19 illustrates the MBV experienced by each semiconductor switch in the proposed twenty-one-level MLI topology. As depicted in the chart, the MBV values vary depending on the switch location within the inverter structure, reflecting the non-uniform voltage stress distribution inherent to the topology. This analysis is crucial for the proper selection of power semiconductor devices, ensuring that each switch can withstand its maximum expected voltage stress under worse-case operating conditions. Furthermore, the identification of these voltage stress levels

facilitates more efficient thermal and insulation design, allowing for better prediction of switching device lifetime and overall system reliability. The presented MBV distribution also serves as a key design consideration in balancing performance with cost, particularly when choosing between devices with varying voltage ratings and switching capabilities.

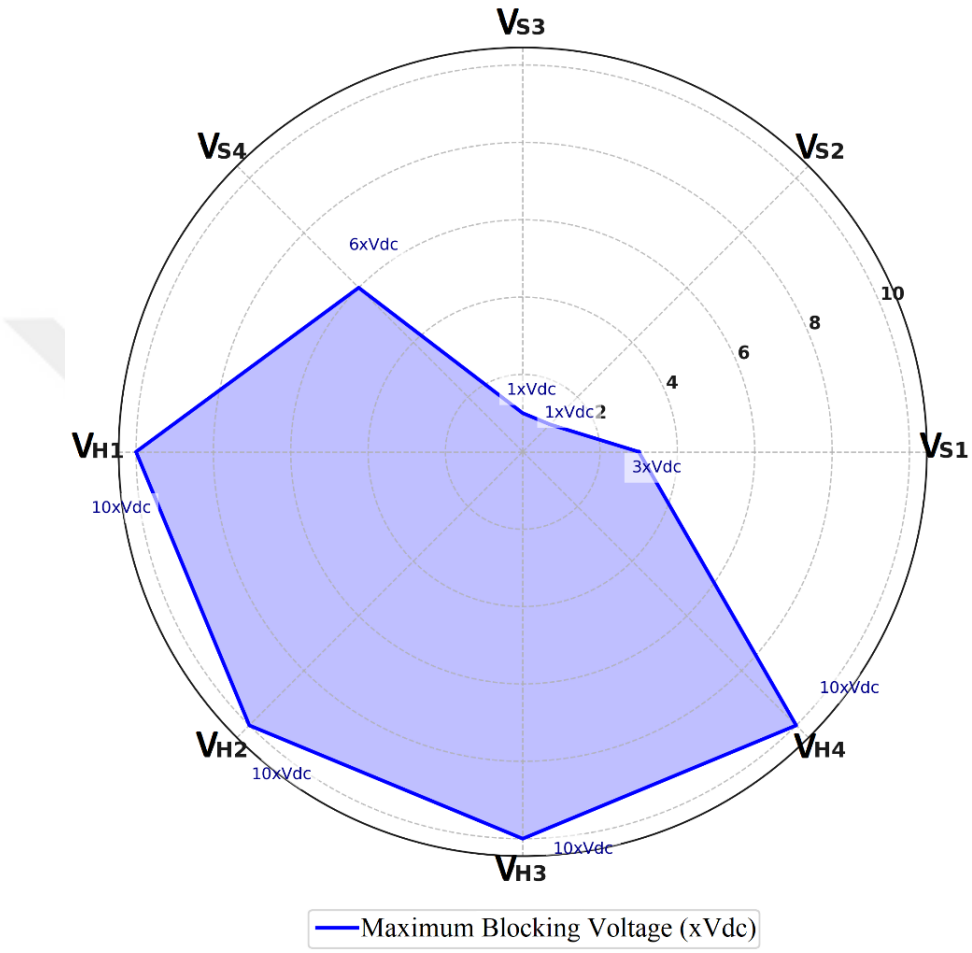


Figure 5.1 MBVs distribution per switch in the proposed twenty-one-level MLI topology

In the analysis of the proposed topology, the voltage stress imposed on each unidirectional switch plays a critical role in device selection and system reliability. With i = 1, 2, 3, … n, the voltage stress experienced by each unidirectional switch corresponds to the voltage level associated with its respective position in the inverter structure. This expression provides a systematic basis for quantifying the MBV experienced by each switch. The following is a detailed representation of the individual voltage stress values across each unidirectional switch, which facilitates

the evaluation of component ratings and supports optimal device allocation within the topology.

$$
\begin{aligned}
MBVs_1 &= V_{S1} = V_2 = 3V_{DC} \\
MBVs_2 &= V_{S2} = V_1 = 1V_{DC} \\
MBVs_3 &= V_{S3} = V_1 = 1V_{DC} \\
MBVs_4 &= V_{S4} = V_3 = 6V_{DC} \\
MBV_{H1} &= V_{H1} = V_1 + V_2 + V_3 = 10V_{DC} \\
MBV_{H2} &= V_{H2} = V_1 + V_2 + V_3 = 10V_{DC} \\
MBV_{H3} &= V_{H3} = V_1 + V_2 + V_3 = 10V_{DC} \\
MBV_{H4} &= V_{H4} = V_1 + V_2 + V_3 = 10V_{DC}
\end{aligned}
$$

In conclusion, the calculation and distribution of MBV for each semiconductor switch provides critical insights into the electrical stress profile of the proposed twenty-one-level MLI topology. These results not only guide the appropriate selection of power devices but also contribute to the optimization of the inverter's overall performance in terms of reliability, cost-efficiency, and thermal management. The identified MBV values confirm the viability of the proposed configuration in minimizing voltage stress disparities among switches, which is essential for balanced operation and extended system lifespan [128].

5.3.3 Total Standing Voltage and Total Standing Voltage per Unit

In MLI systems, TSV refers to the cumulative voltage stress experienced by all semiconductor switches within the converter during its operation. It serves as a key indicator of the overall insulation and voltage-blocking demands within the entire inverter configuration. TSV is directly related to the overall voltage handling capacity and influences both the reliability and cost of the system, as switches with higher voltage ratings are typically more expensive and may exhibit lower switching performance.

To enable fair comparison across different topologies regardless of the number of voltage levels, the TSV_{pu} is introduced. TSV_{pu} normalizes the TSV with respect to the output voltage level, providing a dimensionless indicator of how efficiently a topology utilizes its switches in terms of voltage blocking. A lower TSV_{pu} signifies better voltage utilization, meaning that less redundant voltage stress is distributed across the components, which ultimately contributes to enhanced efficiency, reduced cost, and potentially smaller physical size of the inverter system.

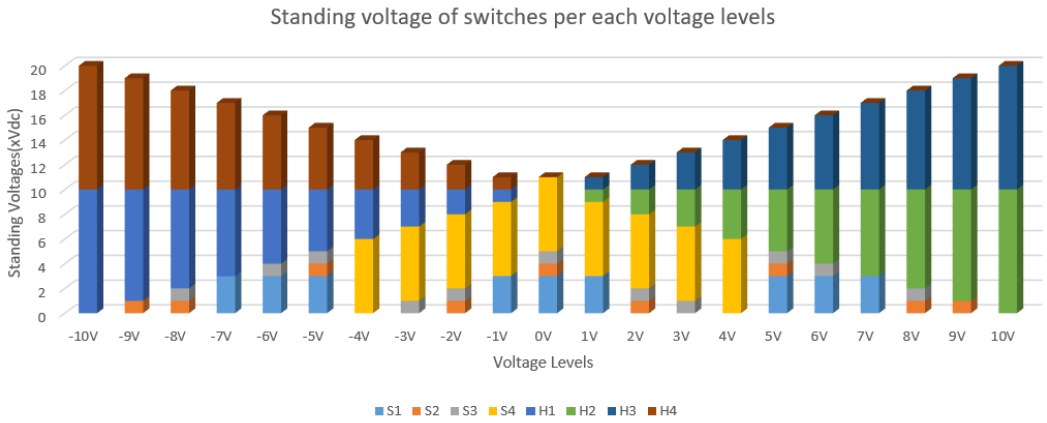


Figure 5.1 Standing voltages of switches per each voltage level in the proposed twenty-one-level MLI topology

To further evaluate the electrical stress imposed on the switching devices, the TSV is computed as the sum of the MBVs of all semiconductor switches within the inverter topology, as previously discussed. Each switch is subjected to a specific voltage stress while in the off state-referred to as its blocking voltage-and TSV represents the cumulative total of these individual stresses. This parameter is fundamental, as it directly affects the selection criteria for power semiconductor devices, which in turn influences both the system cost and its electrical performance. The distribution of these standing voltages across different switches is depicted in Figure 5.20, which provides insight into how voltage stress is shared within the proposed topology.

Given its critical influence on device selection and overall inverter performance, the TSV serves not only as a theoretical construction but also as a practical design criterion. Accordingly, its quantitative assessment is essential for validating the effectiveness of the proposed topology in terms of voltage stress distribution.

A graphical representation of the MBV distribution across all semiconductor switches is provided in Figure 5.19, offering a visual complement to the analytical TSV evaluation discussed earlier. As illustrated, the TSV is determined by summing the MBV values of all switches within the inverter structure. This relationship is formally expressed in equation (5.4), which serves as the basis for the subsequent numerical calculations presented in the following section.

$$TSV = \sum_{i=1}^{n} MBV_{Si} \quad (5.4)$$

$$TSV = MBV_{S1} + MBV_{S2} + MBV_{S3} + MBV_{S4} + MBV_{H1} + MBV_{H2} + MBV_{H3} + MBV_{H4}$$

$$TSV = 3V_{DC} + 1V_{DC} + 1V_{DC} + 6V_{DC} + 10V_{DC} + 10V_{DC} + 10V_{DC} + 10V_{DC} = 51V_{DC}$$

Equation (5.5) defines the TSV_{pu} as the ratio between the overall TSV, and the highest output voltage level achieved by the proposed MLI configuration.

$$TSV_{PU} = \frac{V_{TSV}}{V_{OMAX}} \quad (5.5)$$

The developed topology's maximum output voltage (V_{OMAX}) is calculated as:

$$V_{OMAX} = 10V_{DC}$$

TSV_{PU} is provided by

$$TSV_{PU} = \frac{51}{10} = 5.1$$

This result indicates that the proposed topology imposes a significant voltage blocking requirement on the switching devices; however, this drawback is offset by the achievement of a higher output voltage and a reduced number of components. Therefore, considering the reduction in the number of switches and the improvement in output levels, the proposed configuration offers acceptable performance in terms of TSV [128].

5.3.4 Normalized Voltage Stress

NVS is defined as the ratio of MBV to the total DC link voltage. It provides a dimensionless metric for comparing the voltage stress on individual devices relative to the overall voltage span of the system. Lower NVS values are desirable as they suggest that individual switches operate under less electrical strain, promoting improved efficiency and reliability.

NVS, or the effect of stress distribution on the switches, is computed using the power switches' TSV and MBV values and is shown in Table 5.1. This shows how much stress is distributed throughout the switches. Equation (5.6) is used to compute the voltage stress across a single switch divided by the circuit's maximum stress [129].

$$\text{TSV}_{\text{PU}} = \frac{\text{Actual Voltage Stress Across Switch}}{\text{Maximum Voltage Stress In The Circuit}} \quad (5.6)$$

TABLE 5.1: NVS calculation for the proposed twenty-one-level MLI topology

Switches	MBV (xV_{dc})	NVS	Impact of stress on switches
S_1	$3V_{dc}$	$3V_{dc}$ /$10V_{dc}$	30%
S_2	$1V_{dc}$	$1V_{dc}$ /$10V_{dc}$	10%
S_3	$1V_{dc}$	$1V_{dc}$ /$10V_{dc}$	10%
S_4	$6V_{dc}$	$6V_{dc}$ /$10V_{dc}$	60%
H_1	$10V_{dc}$	$10V_{dc}$ /$10V_{dc}$	100%
H_2	$10V_{dc}$	$10V_{dc}$ /$10V_{dc}$	100%
H_3	$10V_{dc}$	$10V_{dc}$ /$10V_{dc}$	100%
H_4	$10V_{dc}$	$10V_{dc}$ /$10V_{dc}$	100%

MBV, NVS, and the overall contribution of each switch to total stress have all been used to examine the voltage stress distribution across the power switches in the suggested 21-level MLI. The biggest contribution to the overall circuit stress is made by the power switches H_1, H_2, H_3, and H_4, which have a maximum voltage stress of $10V_{dc}$ and an NVS of 100%. With an MBV of $6V_{dc}$ and an NVS of 60%, switch S_4 functions at an intermediate stress level, which is greater than the minimum stress group but far lower than the maximum stress group. With MBVs of $3V_{dc}$, $1V_{dc}$, and $1V_{dc}$, respectively, and NVS values of 30%, 10%, and 10%, switches S_1, S_2, and S_3 experience the least amount of stress.

It is noteworthy that the switches S_1, S_2, S_3, and S_4, which are not part of the H-bridge configuration-unlike H_1, H_2, H_3, and H_4-are exposed to comparatively lower voltage stress levels. As the proposed MLI topology is scaled by incorporating additional units to achieve higher output voltage levels, the NVS values of these non-H-bridge switches are expected to decrease progressively. This behavior stems from the inherent modularity of the topology, where added submodules contribute to voltage level generation in a distributed manner. As a result, the voltage stress is shared among a greater number of auxiliary switches, thereby reducing the individual stress on each. This characteristic not only enables the use of lower voltage-rated and cost-effective semiconductor devices for non-H-bridge positions but also enhances the scalability and economic feasibility of the overall inverter design.

In conclusion, the voltage stress analysis of the proposed twenty-one-level MLI topology reveals a distinct distribution pattern. Due to their fundamental role in generating full-level bipolar output voltage, only the H-bridge switches (H_1-H_4)

consistently experience maximum voltage stress, resulting in NVS values approaching 100%. In contrast, the remaining switches exhibit significantly lower NVS values, which further decline as the number of voltage levels increases. This divergence in stress distribution emphasizes the effectiveness of the topology in managing voltage stress asymmetrically across the switching devices. Ultimately, this approach allows for a hybrid design utilizing switches with varying voltage ratings, thus ensuring both cost-efficiency and robust performance in high-level inverter applications [129].

5.3.5 Cost Function and Cost Function per Level

The CF serves as a consolidated metric that integrates the expenses of critical components-such as power switches, gate driver circuits, diodes, capacitors, and DC sources-into a single quantitative framework, effectively representing the overall economic footprint of a given inverter topology. When normalized by the number of output voltage levels, the CF/L emerges as a scalable index, enabling fair and consistent comparisons among various MLI configurations. Lower CF and CF/L values are indicative of enhanced cost efficiency, thereby positioning these metrics as essential decision-making tools, particularly in cost-sensitive applications.

In this context, the proposed twenty-one level MLI topology is evaluated with respect to its overall cost and structural complexity by employing the CF as a principal criterion. The assessment considers the number of vital components, including switches (N_{SW}), N_{dc}, number of diodes (N_d), number of capacitors (N_c), and gate driver circuits (N_{gd}), all of which contribute directly to the material cost and implementation complexity. Notably, the number of switches significantly influences not only the hardware cost but also the complexity of the control circuitry. Similarly, the inclusion of multiple DC sources and capacitors impacts both the total expenditure and the physical footprint of the inverter system, as each component introduces additional challenges in design optimization and power management.

The CF is formulated as a function (5.7) incorporating the total number of key components, as shown below:

$$CF = (N_{sw} + N_{dc} + N_{gd} + N_d + N_C + \alpha \times TSV_{pu}) \times n \quad (5.7)$$

Here, α is a weighting coefficient introduced to adjust the influence of the TSV_{PU} on the overall cost. Its value is typically chosen based on system-specific requirements, with lower values (e.g., α=0.5) used when the influence of TSV is considered less critical, and higher values (e.g., α=1.5) applied when greater emphasis on voltage stress is needed. Also, in the equation, n is the number of DC voltage sources. In this study, these values were selected accordingly to reflect the appropriate trade-off between economic and performance considerations in cost evaluation.

Before presenting the numerical results for the proposed 21-level MLI topology, it is important to apply the CF formulation to the specific component counts of the design. This enables a detailed comparison with alternative topologies in terms of cost-efficiency and implementation feasibility.

For the proposed topology, the number of switches, DC voltage sources, gate driver circuits, diodes, capacitors and TSV_{pu} are given respectively as follows: $N_{SW} = 8$, $N_{dc} = 3$, $N_{gd} = 8$, $N_d = 4$, $N_c = 0$ and α x $TSV_{pu} = 2.55$ (if α = 0.5) or 5.1 (if α = 1).

According to equation 7, the CF is calculated as follows:

$$CF = (8+3+8+4+0+2.55)\times 3 = 67.65(if\ \alpha = 0.5)$$
$$CF = (8+3+8+4+0+7.65)\times 3 = 82.95(if\ \alpha = 1.5)$$

The equation (5.8) is employed to calculate the CF/L value.

$$CF/L = \frac{CF}{N_{level}} \quad (5.8)$$

The CF per level calculation for the proposed 21-level topology has been carried out as demonstrated below.

$$CF/L = \frac{67.65}{21} = 3.22 (\text{if } \alpha = 0.5)$$
$$CF/L = \frac{82.95}{21} = 3.95 (\text{if } \alpha = 1.5)$$

In conclusion, the CF and CF/L metrics are critical for assessing the cost-efficiency dimension of system performance. According to the results obtained, the CF value is 23.55 and the CF/L ratio is 1.12 when α = 0.5. For α = 1.5, these values increase to 28.65 and 1.36, respectively. These numerical outcomes indicate that the system

maintains an acceptable and stable cost level even under varying α parameters. Notably, the relatively low CF/L ratios suggest that the system ensures efficient resource utilization and remains scalable. Furthermore, the limited variation in these metrics with respect to changes in α highlights the robustness and cost-effectiveness of the proposed approach across different scenarios.

In this context, incorporating cost-oriented indicators such as CF and CF/L into the analysis process is crucial for ensuring economic efficiency in system design and for guiding decision-making processes in a rational and data-driven manner. Considering these parameters during the analysis phase allows for a more comprehensive assessment of the system from both technical and economic perspectives [128], [130].

5.3.6 Component Level Factor

One of the key performance indicators used to evaluate and compare the structural efficiency of MLI topologies is the F_{ccl}. This factor is defined as the ratio of the total number of components utilized in the topology to the number of generated output voltage levels. Topologies that achieve higher voltage levels with fewer components are considered more advantageous. The calculation of F_{ccl} for the proposed topology has been carried out using the mathematical expression provided below to assess its structural efficiency.

Equation (5.9) is used to compute the component level factor.

$$F_{ccl} = \frac{N_{sw} + N_{d} + N_{cap} + N_{gd} + N_{dc}}{N_{level}} \quad (5.9)$$

The F_{ccl} value for the proposed topology has been calculated using Equation (5.9), and the corresponding computation is presented below.

$$F_{ccl} = \frac{8+4+0+8+3}{21} = \frac{23}{21} = 1.09$$

The calculated F_{ccl} value for the proposed topology is found to be 1. This result indicates that only one component is required per output voltage level, which reflects a highly efficient structural design. Such a low F_{ccl} value contributes not only to reduced system complexity but also to lower cost and compactness. Furthermore, as additional modular units are integrated into the topology to increase

the number of output voltage levels, the F_{ccl} value decreases even further. This reduction becomes particularly significant at higher levels, offering a dramatic improvement in structural efficiency. Therefore, the proposed configuration can be considered a highly competitive alternative, especially in applications demanding many output levels [130].

6
RESULTS AND DISCUSSION

This chapter presents a comprehensive analysis of the simulation results obtained from the proposed asymmetric twenty-one level MLI. The performance of the topology is evaluated based on various criteria, including output voltage waveform quality, harmonic distortion levels, power loss trends, and overall system efficiency. The results are not only interpreted in isolation but also benchmarked against conventional inverter configurations to highlight the relative advantages and trade-offs associated with the proposed design.

Initially, the simulated output voltage and current waveforms are examined under representative load conditions to verify proper voltage level generation and switching logic. Subsequently, a detailed harmonic spectrum analysis is performed to quantify the THD and assess waveform purity. The chapter further investigates conduction and switching losses, offering insights into the thermal and energy performance of the system. Finally, a comparative study is presented where key metrics such as THD, switching device stress, and component count are contrasted with those of benchmark topologies, demonstrating the effectiveness and innovation of the proposed solution.

6.1 Simulation Results

Figures 6.1 and 6.2 illustrate the output voltage waveform of a 21-level MLI topology under different loading conditions, compared against an ideal sinusoidal reference waveform. In Figure 6.1, the inverter is connected to a purely R load. Under this condition, the output voltage (blue waveform) closely follows the sinusoidal reference (green waveform), with clearly defined voltage steps. The high resolution of these steps indicates effective level synthesis, resulting in low THD.

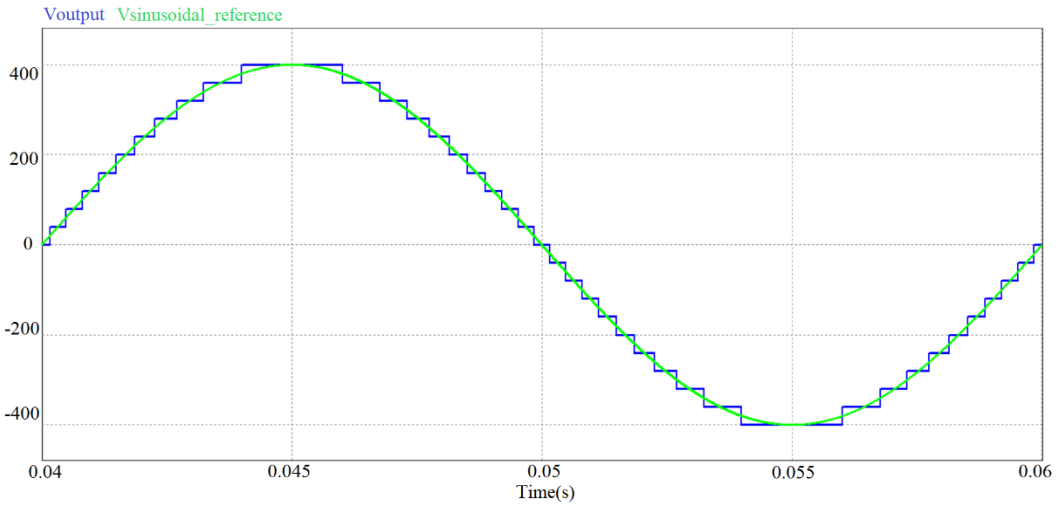


Figure 6.1 Comparison of output voltage under R load and sinusoidal reference

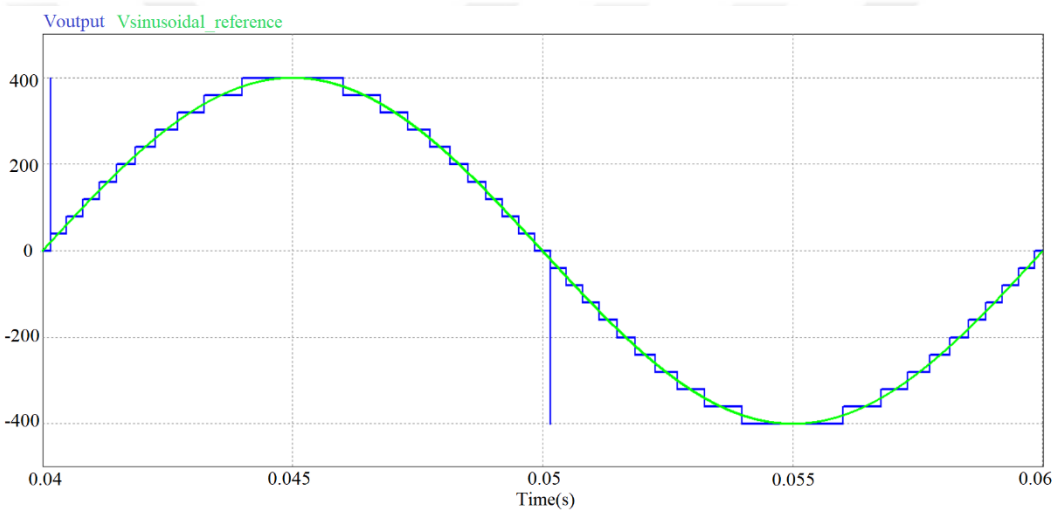


Figure 6.2 Comparison of output voltage under RL load and sinusoidal reference

In contrast, Figure 6.2 illustrates the inverter's output under a RL load condition. The inductive component introduces a phase difference between voltage and current, leading to transient effects during switching transitions. These effects are particularly noticeable around t = 0.05 s, where the output waveform exhibits sharp voltage spikes and discontinuities. Such disturbances are primarily caused by the inductor's stored energy, which generates a back electromotive force that interferes with the switching process and results in over voltages.

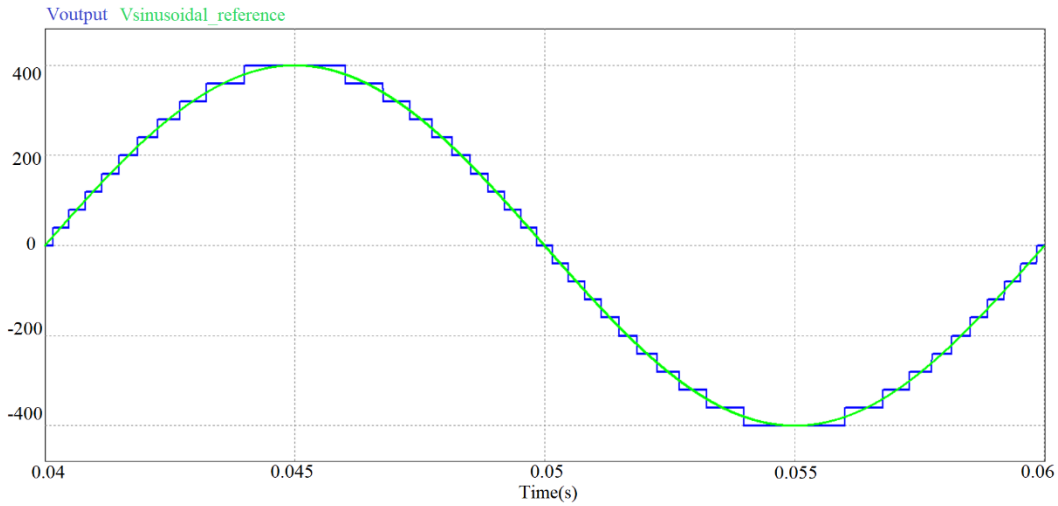


Figure 6.3 Comparison of output voltage under RL load with turn-off snubbers and sinusoidal reference

To address these issues, Figure 6.3 shows the output voltage under the same RL load, but this time with turn-off snubber circuits implemented. The comparison reveals that the previously observed voltage spikes in Figure 6.2 have been effectively suppressed. The waveform in Figure 6.3 demonstrates significantly improved conformity to the sinusoidal reference, indicating that the turn-off snubber successfully mitigates the transient over voltages caused by the inductive load.

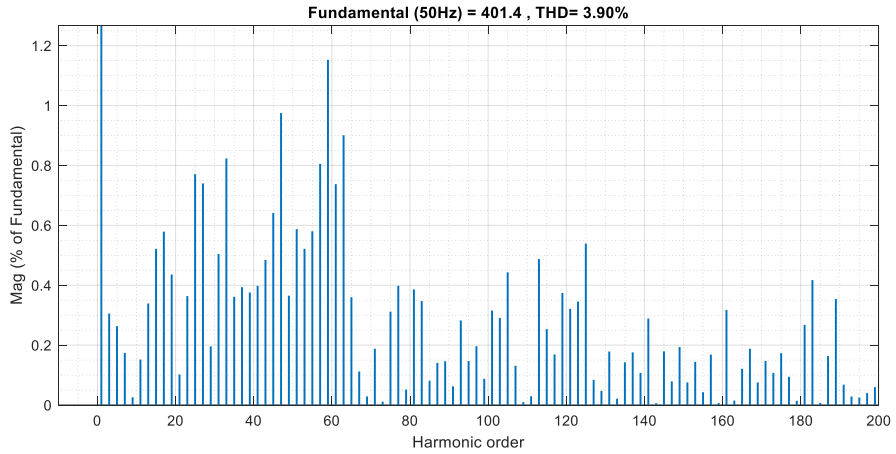


Figure 6.4 FFT analysis of the proposed twenty-one-level output voltage waveform with RL load including snubber circuit (up to the 200th harmonic order)

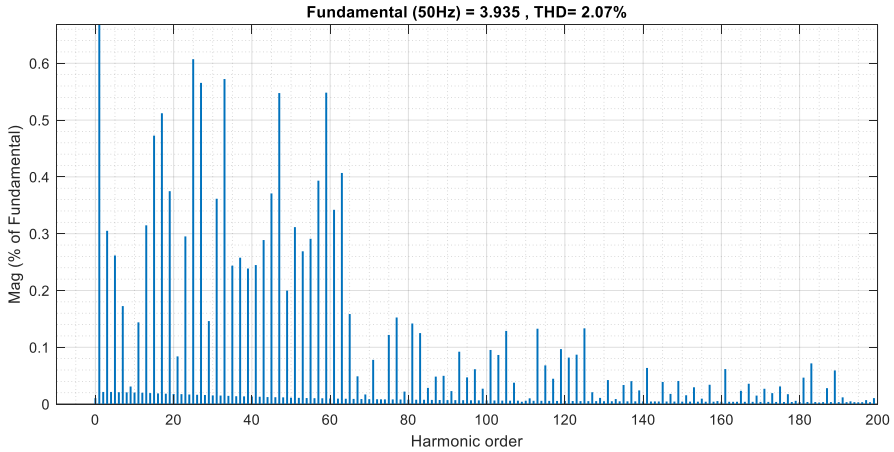


Figure 6.5 FFT analysis of the proposed twenty-one-level output current waveform with RL load including snubber circuit (up to the 200th harmonic order)

The frequency spectra of the output voltage and output current waveforms of the suggested 21-level inverter topology with a snubber circuit under RL load are shown in Figures 6.4 and 6.5 up to the 200th harmonic order. Harmonic amplitudes above the fundamental component are found to be considerably diminished. This demonstrates that snubber-assisted switching improves the system's electromagnetic compatibility and the waveforms' spectrum purity.

The usefulness of the suggested snubber design in real-world power electronics applications is confirmed by the resulting harmonic profile, particularly in grid-connected systems where low THD is a crucial requirement. These results confirm that it is both theoretically sound and practically feasible to incorporate passive protection components into the inverter design. Additionally, the analysis's spectrum performance shows that it complies with IEEE 519 criteria [131].

In summary, the use of turn-off snubbers ensures smoother voltage transitions, enhances waveform fidelity, and protects the switching devices from potentially damaging voltage overshoots. This validates the critical role of passive protection circuits in inverter designs, particularly when inductive components are present in the load.

6.2 Advantages over Conventional Topologies

A systematic comparison of MLI topologies is essential for identifying configurations that offer optimal trade-offs between performance, complexity, and cost. Conventional topologies such as the CHB, NPC, and FC have long been

recognized for their effectiveness; however, they often suffer from inherent limitations related to high component count, increased control burden, and reduced scalability. The proposed topology seeks to overcome these drawbacks by introducing a structurally simplified alternative that achieves the desired number of voltage levels with significantly fewer active and passive components. This reduction directly translates to improved efficiency, compactness, and cost-effectiveness.

In this section, the proposed topology is analytically compared to its conventional counterparts using a broad set of technical and economic performance indicators. The analysis not only highlights key design efficiencies but also substantiates the proposed approach as a viable candidate for advanced MLI applications.

Table 6.1 offers a comprehensive evaluation of various multilevel converter topologies by examining a range of performance parameters. The N_{level} represents the granularity of the output voltage waveform, where a higher-level count typically correlates with improved waveform quality at the expense of increased circuit complexity. The N_{sw} and N_{gd} denote the required semiconductor devices and their associated control units, both of which significantly influence the overall system cost, power efficiency, and spatial footprint. The N_{dc} provides insight into the topology's power input requirements, whereas the N_d and N_c reflect the necessity for auxiliary components such as clamping elements and energy storage units. To assess circuit complexity in relation to output resolution, the F_{ccl} metric is used, indicating the average number of components utilized per voltage step. TSV_{pu} quantifies the aggregate voltage stress endured by all circuit components, normalized per unit, serving as a critical measure of system robustness and cost implications. Lastly, the CF/L provides a measure of economic efficiency for each topology, calculated under two distinct weighting coefficients ($\alpha = 0.5$ and $\alpha = 1.5$), thereby illustrating the sensitivity of cost optimization to design priorities [130].

Additionally, favorable values for F_{ccl} indicate reduced circuit complexity and voltage stress, contributing to improved compactness and reliability. The CF results under both weighting scenarios further underscore the economic advantages of the proposed design, confirming its potential as a practical and scalable solution for medium- and high-power applications.

TABLE 6.1: Comparative evaluation of the proposed twenty-one-level MLI topology against conventional MLI configurations

Topologies/ Parameters	CHB	NPC	FC	Proposed Topology
N_{level}	21	21	21	21
N_{sw}	40	40	40	8
N_{gd}	40	40	40	8
N_{dc}	10	1	1	3
N_{d}	12	20	10	4
N_{c}	3	20	20	0
F_{ccl}	5	5.76	5.28	1.1
TSV_{pu}	4	4	4	5.1
CF/L (α =0.5)	46.19	5.81	5.33	3.22
CF/L (α =1.5)	48.09	6	5.52	3.95

The comparative analysis presented in Table 6.1 highlights the technical and economic superiority of the proposed twenty-one-level MLI topology over conventional configurations, including CHB, NPC, and FC topologies. The proposed design achieves notable reductions in component count and control complexity while maintaining or surpassing key performance metrics, making it a strong candidate for high-performance and cost-sensitive power electronics applications.

One of the most significant improvements is observed in the N_{sw} and the associated N_{gd}. While all conventional topologies utilize 40 switches and 40 gate drivers to achieve a 21-level output, the proposed topology accomplishes the same level count with only 8 switches and 8 gate driver circuits. This corresponds to an 80% reduction in switch count and an 85% reduction in driver circuitry, leading to substantially lower power losses, simpler control strategies, and minimized system volume and cost. These reductions not only improve system efficiency but also reduce the risk of fault propagation and enhance reliability.

Furthermore, the N_{dc} required by the proposed topology is limited to 3, as opposed to the 10 sources used in CHB or the single-source structure in NPC and FC. While NPC and FC benefit from single-source operation, they suffer from significantly higher N_d and N_c-reaching up to 20 components in either category. In contrast, the proposed topology uses only 4 diodes and eliminates the need for capacitors entirely, thereby simplifying circuit construction and reducing passive component-related losses, costs, and design constraints.

In terms of F_{ccl}, which is a crucial indicator of circuit modularity and scalability, the proposed topology achieves a value of 1.1, indicating minimal hardware requirements per voltage level. Conventional topologies, by comparison, exhibit values ranging from 5.0 to 5.76. This drastic simplification facilitates easier implementation, fault diagnosis, and maintenance, while supporting higher voltage level scalability with reduced incremental cost.

While the TSV_{pu} for the proposed inverter is slightly higher at 5.1, compared to 4.0 in conventional alternatives, this increase is modest and justifiable considering the substantial component savings and reduced system complexity. Moreover, the higher TSV_{pu} can be mitigated through optimized component selection and layout strategies.

Most notably, the CF/L-a comprehensive metric that encapsulates the trade-off between performance and economic factors-demonstrates the economic efficiency of the proposed topology. Under two distinct weighting scenarios ($\alpha = 0.5$ and $\alpha = 1.5$), the proposed inverter records the lowest values of 3.22 and 3.95, respectively. These results underscore the proposed design's remarkable cost-performance balance and its suitability for both low-cost and high-reliability applications.

In conclusion, the proposed topology not only meets the functional and performance requirements for a 21-level inverter but does so with unprecedented efficiency in terms of component utilization, control effort, and cost structure. These characteristics affirm their potential as a superior alternative to traditional MLI architectures, particularly in applications demanding compactness, modularity, and cost-effectiveness.

6.3 Comparison with Benchmark Topologies

This section presents a performance comparison between the proposed 21-level MLI topology and six widely recognized benchmark topologies from the literature. The comparison is based on key structural and performance parameters including the N_{sw}, N_{gd}, N_{dc}, N_d, and N_c, as well as F_{ccl}, TSV_{pu}, and CF/L.

TABLE 6.1: Comparative evaluation of the proposed twenty-one-level MLI topology against another RSC-MLIs

Topologies/ Parameters	**[132]**	**[133]**	**[134]**	**[135]**	**[136]**	**[137]**	**Proposed Topology**
$\mathbf{N_{level}}$	21	21	21	21	21	21	**21**
$\mathbf{N_{sw}}$	10	12	16	10	10	14	**8**
$\mathbf{N_{gd}}$	10	10	16	10	10	14	**8**
$\mathbf{N_{dc}}$	3	3	7	6	4	3	**3**
$\mathbf{N_d}$	0	0	0	10	0	3	**4**
$\mathbf{N_c}$	0	0	0	3	0	3	**0**
$\mathbf{F_{ccl}}$	1.1	1.2	1.86	1.86	1.14	1.76	**1.1**
$\mathbf{TSV_{pu}}$	4	4.4	6.7	4	6.2	6.2	**5.1**
CF/L (α =0.5)	3.14	3.45	11.78	10	4.4	5.3	**3.22**
CF/L (α =1.5)	3.71	4.08	14.01	11.14	5.58	6.18	**3.95**

As summarized in Table 6.2, the proposed topology demonstrates significant advantages by requiring fewer switching devices and gate drivers, thereby reducing system complexity and cost. Furthermore, the proposed configuration achieves competitive performance in terms of total voltage stress and CF metrics.

The table compares various MLI topologies, including a proposed topology, in terms of key parameters such as the N_{level}, N_{sw}, N_{gd}, N_{dc}, N_d, N_c, F_{ccl}, TSV_{pu}, and CF/L for two weighting factors, ($\alpha = 0.5$) and ($\alpha = 1.5$).

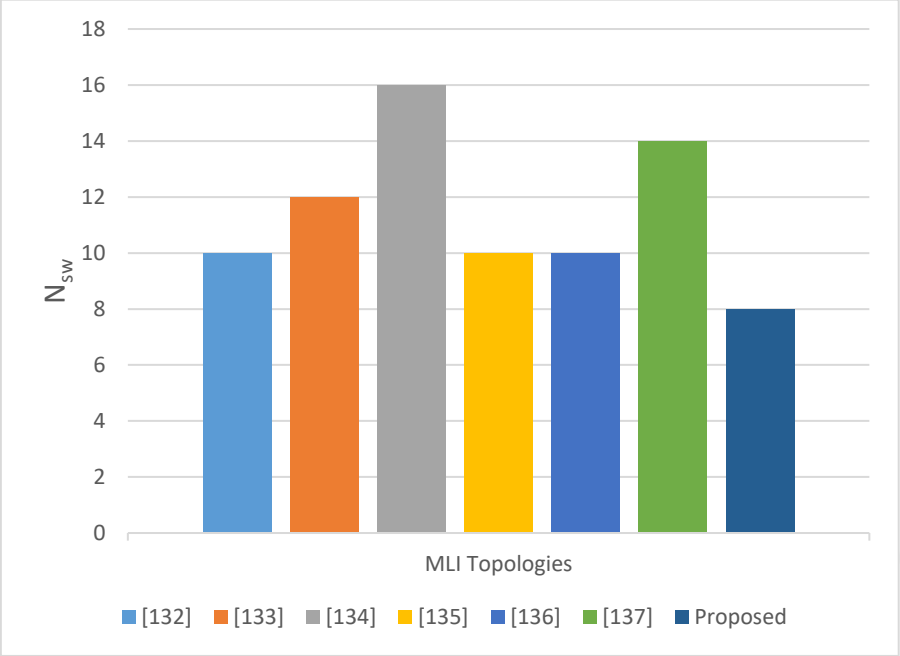


Figure 6.1 Comparison of the proposed topology with existing MLI topologies in terms of the number of switching devices

As illustrated in Figure 6.6, the proposed MLI topology significantly reduces the number of switching devices compared to conventional designs. While existing MLI topologies typically employ 10 to 16 switches, the proposed configuration requires only 8 switches, indicating superior optimization. This reduction in the N_{sw} not only minimizes conduction and switching losses but also contributes to a simpler circuit structure and lower implementation cost.

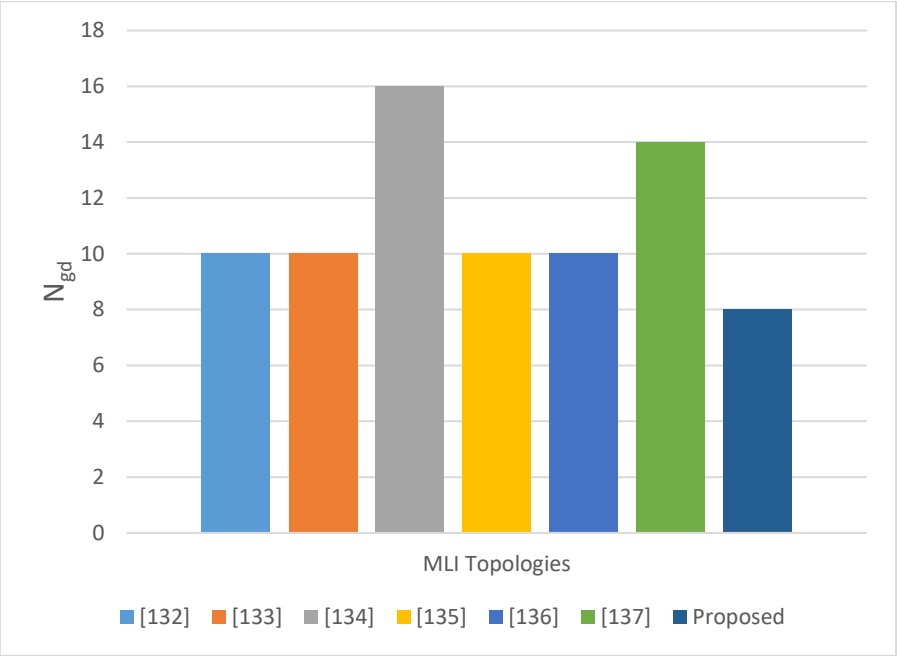


Figure 6.2 Comparison of the proposed topology with existing MLI topologies in terms of the number of gate driver devices

As shown in Figure 6.7, the proposed topology significantly reduces the N_{gd} required for operation. In conventional MLI designs, the number of gate drivers typically matches the number of switches, ranging from 10 to 16. In contrast, the proposed configuration requires only 8 gate driver circuits, demonstrating improved efficiency in minimizing the need for auxiliary components. This reduction contributes to simpler gate control circuitry, lower cost, and improved system reliability.

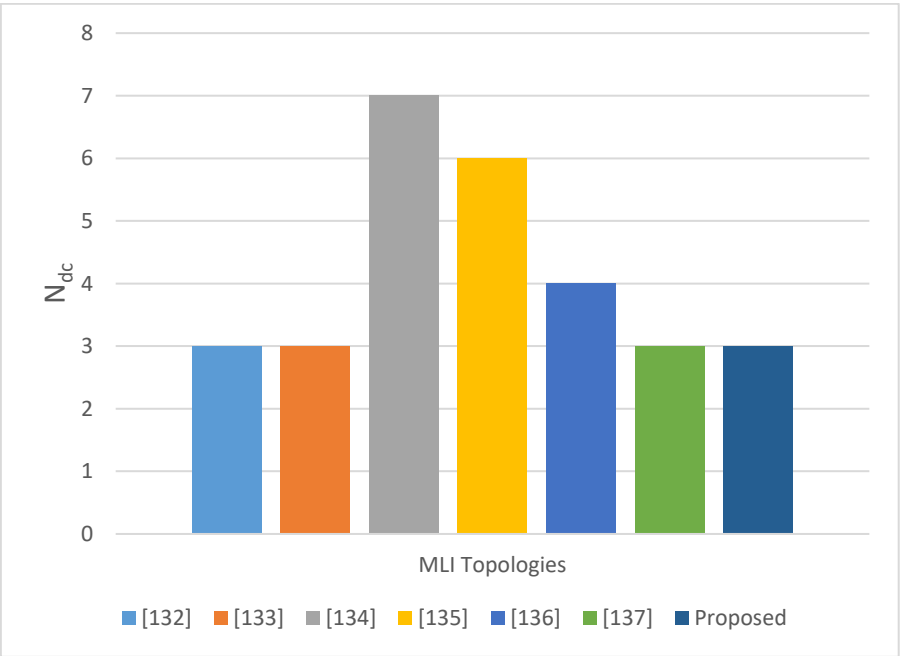


Figure 6.3 Comparison of the proposed topology with existing MLI topologies in terms of the number of voltage sources

As illustrated in Figure 6.8, the proposed MLI topology employs three N_{dc}, which is comparable to the most efficient existing topologies that also utilize three sources. The number of DC sources directly affects the complexity and cost of power supply management. By maintaining this number at an optimized level, the proposed design achieves a favourable trade-off between system performance and implementation complexity, ensuring high efficiency without introducing additional cost burdens.

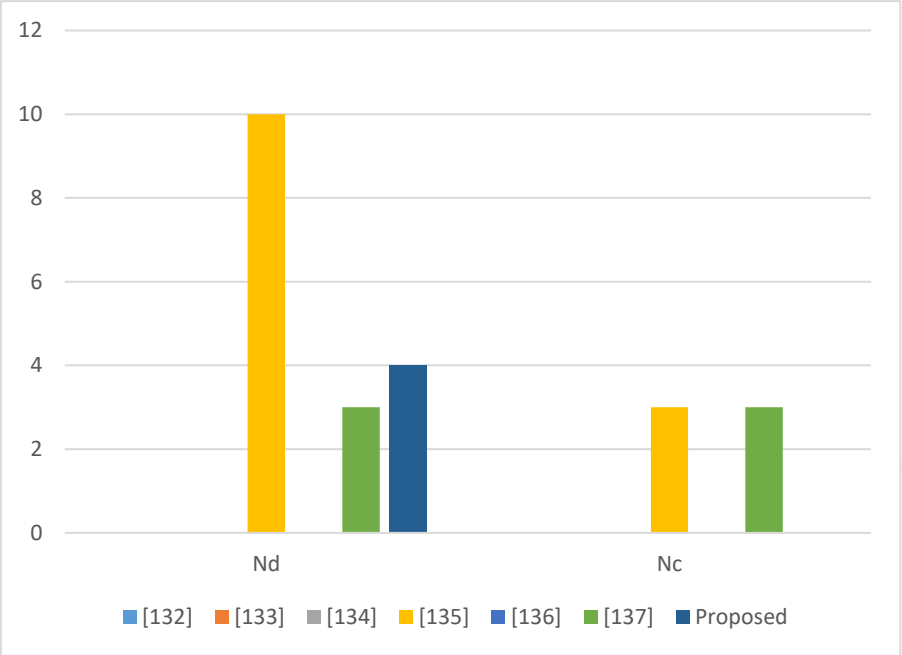


Figure 6.4 Comparison of the proposed topology with existing MLI topologies in terms of the number of diodes and capacitors

As presented in Figure 6.9, the proposed MLI topology differs from existing designs in terms of passive component requirements, particularly diodes and capacitors. Regarding the N_d, the proposed topology includes 4 diodes, whereas most conventional designs operate without any diodes. Although diodes may increase conduction losses and system complexity, their inclusion in this design likely serves a targeted function-such as enhancing voltage balancing or improving operational reliability.

In terms of the N_c, the proposed topology stands out by completely avoiding the use of capacitors, like certain efficient designs in the literature. In contrast, some existing topologies utilize up to 10 capacitors, which can increase system cost,

volume, and control complexity. Thus, by minimizing both diode and capacitor usage, the proposed topology offers a compact, low-loss, and cost-effective solution.

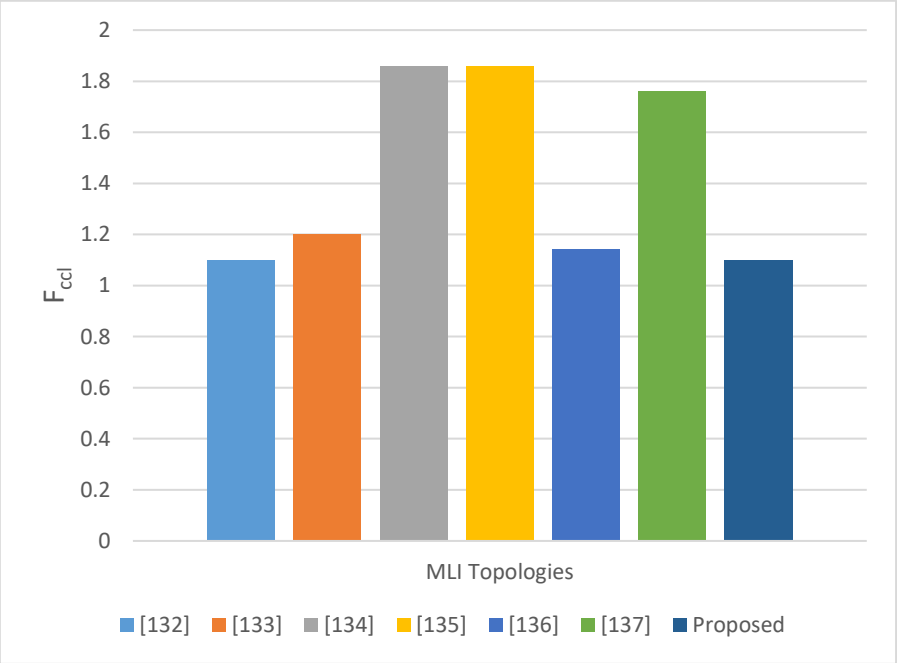


Figure 6.5 Comparison of the proposed topology with existing MLI topologies in terms of the F_{ccl}

The efficiency of the proposed topology in terms of component usage can be clearly observed in Figure 6.10, which compares the F_{ccl} across various MLI topologies. The proposed design achieves an F_{ccl} value of 1.1, which is notably lower than all existing topologies, whose values range between 1.1 and 1.86. This significant reduction demonstrates the compactness and efficiency of the proposed topology, as it requires fewer components to achieve the same number of voltage levels.

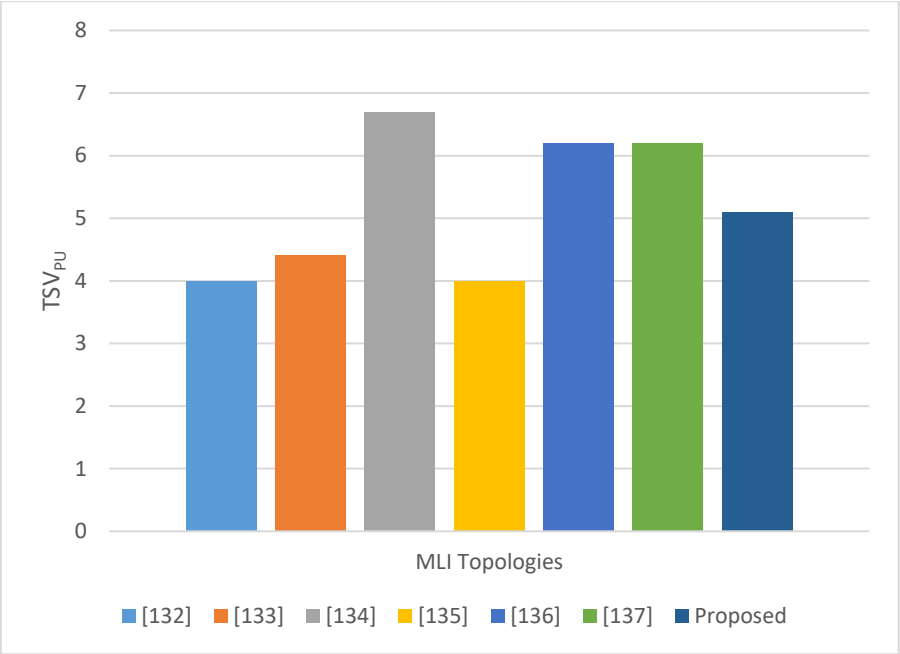


Figure 6.6 Comparison of the proposed topology with existing MLI topologies in terms of the TSV_{pu}

The TSV_{pu} is a critical parameter that affects both the reliability and physical dimensions of inverter components. As illustrated in Figure 6.11, the proposed topology achieves a TSV_{pu} value of 5.1. While this value is higher than those reported in [133] and [134], it remains lower than the value presented in [135]. This positioning indicates a balanced trade-off, where the proposed topology moderately increases voltage stress in favor of reducing component count and achieving overall design optimization.

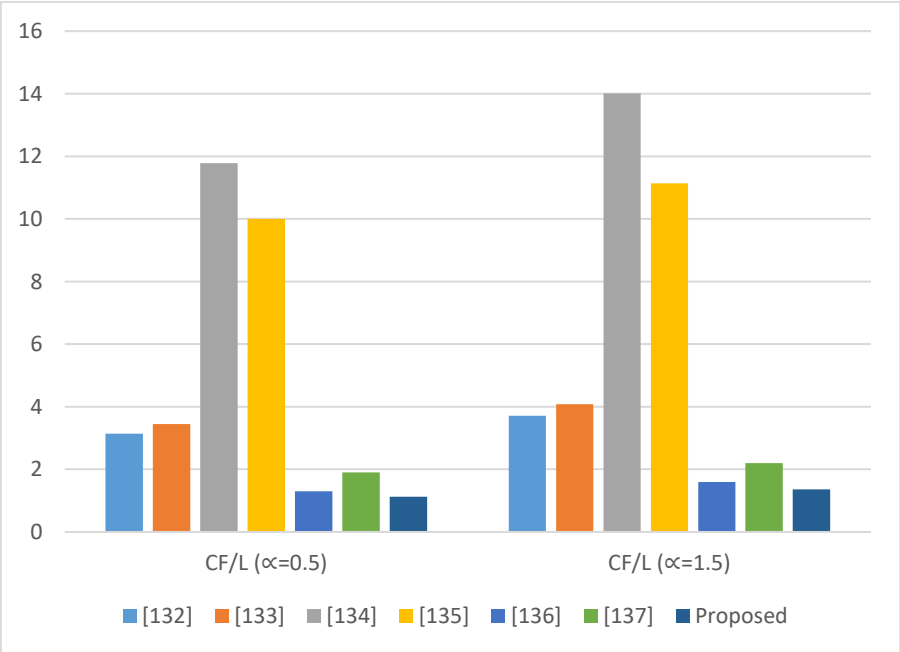


Figure 6.7 Comparison of the proposed topology with existing MLI topologies in terms of the CF/L

The CF/L serves as a key indicator for evaluating the economic efficiency of MLI topologies. As shown in Figure 6.12, the proposed topology achieves a CF/L value of 1.12, which is substantially lower than those of existing topologies, whose values range between 1.3 and 11.78. Furthermore, in another cost metric, the proposed topology attains a value of 1.36, again significantly outperforming other designs, which vary from 1.6 to 14.01. These findings underline the remarkable cost-effectiveness of the proposed topology, demonstrating its superiority in terms of both performance and economic viability.

7
CONCLUSION

This concluding chapter encapsulates the primary outcomes, contributions, and This chapter concludes the research conducted on the design, simulation, and evaluation of a novel asymmetric twenty-one-level MLI topology, emphasizing its performance, contributions, limitations, and directions for future work. The study aimed to introduce a structurally simplified and cost-efficient solution capable of generating high-resolution stepped voltage waveforms while minimizing switching losses and harmonic distortion. In the context of contemporary power electronics, the proposed topology effectively responds to the increasing demand for compact, reliable, and efficient MLIs suitable for medium- and high-power applications such as electric drives, renewable energy systems, and smart grid interfaces.

The proposed topology successfully demonstrates the generation of twenty-one voltage levels using a reduced number of active switches and DC sources in comparison to conventional structures. Through the strategic use of asymmetric voltage sources and an NLC modulation strategy, the inverter achieves significant improvements in waveform quality with minimized THD. Simulation results under both R and RL load conditions confirm the inverter's capacity to closely track a reference sinusoidal voltage waveform.

A comprehensive set of performance metrics was applied to evaluate the topology, including TSV, MBV, NVS, and CF. The proposed topology yielded a CF/L value of 3.22, positioning it among the most cost-effective solutions in the literature, while achieving a TSV_{pu} of 5.1, reflecting a favorable balance between component voltage stress and design compactness. Additionally, F_{ccl} was calculated to be 1.1, indicating exceptional component efficiency per output level.

An important characteristic of the proposed topology is its operation at fundamental switching frequency, enabled by the NLC modulation strategy. This not only minimizes switching losses but also eliminates the need for high-frequency PWM-based control, reducing thermal stress and enhancing overall efficiency. These attributes make the topology particularly attractive for implementation in thermally

constrained environments or applications where passive cooling and simplified gate driver circuitry are desired.

This thesis has contributed several key advancements to the field of MLI technology:

1. Topology Innovation: A new asymmetric inverter structure capable of generating 21 discrete voltage levels using only three asymmetrical DC sources and a RSC-MLI was introduced. This results in both hardware simplification and cost minimization.
2. Switching Strategy: The employment of NLC enabled the system to function at fundamental switching frequency, reducing switching losses and control complexity while ensuring high-quality output waveforms.
3. Harmonic and Efficiency Optimization: By maintaining THD below critical thresholds and optimizing TSV and MBV metrics, the proposed design demonstrates excellent harmonic performance and robustness under varying load conditions.
4. Comparative Benchmarking: The study conducted extensive comparative analysis against several well-established MLI topologies. Results indicated that the proposed inverter outperforms many existing designs in terms of component count, harmonic distortion, and cost efficiency, confirming its practical relevance in the domain of RSC-MLIs.
5. Modularity and Scalability: Though compact, the proposed architecture lends itself to modular implementation, facilitating ease of extension or integration into larger inverter networks such as modular CHB structures or hybrid multilevel configurations.

While the simulation-based results are promising, the research is subject to several limitations:

- Hardware Validation: All performance analyses were limited to PSIM and MATLAB/SIMULINK simulation environments. Experimental hardware implementation is required to confirm system behavior under real-world non-idealities, including switching losses, device delays, parasitic effects, and thermal drift.

- Ideal Switching Conditions: The model assumes idealized switching behavior. Factors such as dead-time effects and nonlinear magnetic behavior of inductive loads were not considered.
- Static Load Conditions: Dynamic or time-varying load behaviors were not deeply investigated. Future studies should incorporate load perturbations and regenerative modes, particularly for EV or motor drive applications.
- Limited Fault Tolerance: The current design does not include active fault detection or self-healing mechanisms. These features are critical for grid-tied or safety-critical environments.
- EMI and Thermal Effects: EMI, insulation coordination, and thermal management strategies were outside the scope of this study and warrant detailed attention in subsequent work.

In summary, the proposed twenty-one-level asymmetric MLI topology offers a promising pathway toward cost-effective, compact, and scalable power conversion systems. By combining architectural simplicity with effective modulation and high-quality waveform synthesis, this study bridges a critical gap between theoretical design and practical applicability in the field of multilevel power electronics. While further experimental validation and application-specific refinements are necessary, the outcomes of this work lay a strong foundation for the development of next-generation inverters tailored to the evolving demands of smart, efficient, and sustainable energy systems.

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PUBLICATIONS FROM THE THESIS

Conference Papers

1. M. Yalçin, S. Özçıra Özkılıç, "AZALTILMIŞ ANAHTAR SAYILI ÇOK SEVİYELİ EVİRİCİLER: ORTA VE YÜKSEK GÜÇ UYGULAMALARINDA TOPOLOJİK GELİŞMELER, MODÜLASYON TEKNİKLERİ, PERFORMANS OPTİMİZASYONU ÜZERİNE BİR İNCELEME," 13. Uluslararası Mühendislik ve Teknoloji Yönetimi Kongresi, pp. 311-318, 2025