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DC-DC SEPIC CONVERTER DESIGN FOR ENERGY HARVESTING APPLICATIONS

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MASTER OF SCIENCE THESIS

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A thesis submitted by Ismail GUZELTEPE in partial fulfillment of the requirements for the degree of **MASTER OF SCIENCE** is approved by the committee on 25.05.2021 in Department of Electronics and Communication Engineering, Electronics Program.

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İsmail GÜZELTEPE

Signature

Dedicated to all women
who warm our hearts with mercy and love.

ACKNOWLEDGEMENTS

My fundamental motivation for this thesis is to make a modest contribution for a greener world by means of designing environmentally harmless systems those do not need conventional batteries endangering our future. I will accept this work as a milestone and I will endeavor to work in accordance with environmental values in the future.

I would like to state my sincere thanks to my advisor Asst. Prof. Dr. Revna Acar VURAL, who is an intellectual scientist of this distinguished university, for her valuable and continuous efforts to support me both motivational and academic means. I am also deeply grateful to Asst. Prof. Dr. Okan Zafer BATUR for supporting me with his knowledge and precious experience and Research Assistant Ö. Faruk GÖKSU for his valuable contributions.

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LIST OF SYMBOLS

V_D	Diode Voltage
$R_{DS,on}$	Drain-Source "On" Resistance
Q	Electric Charge
V_{in}	Input Voltage
KHz	Kilohertz
$V_{in,\min}$	Minimum Input Voltage
V_{out}	Output Voltage
Ω	Resistance
f_{sw}	Switching Frequency
V_s	Source Voltage
V_T	Threshold Voltage
ΔV	Voltage Ripple

LIST OF ABBREVIATIONS

BPW	Buried-P-Well
CISM	Complete Inductor Supply Mode
CCM	Continuous Conduction Mode
CP	Charge Pump
DC/DC	Direct Current to Direct Current
DCM	Discontinuous Conduction Mode
DIDO	Dual Input Dual Output
EH	Energy Harvesting
IISM	Incomplete Inductor Supply Mode
IC	Integrated Circuit
IOT	Internet of Things
MEMS	Micro-Electro-Mechanical Systems
MFC	Microbial Fuel Cells
PV	Photovoltaic
TE	Thermoelectric
PMU	Power Management Unit
SEPIC	Single Ended Primary Inductor Converter
SPC	Switch Peak Current
TEG	Thermoelectric Generator
UMC	United Microelectronics Corporation
WSN	Wireless Sensor Network
ZVS	Zero Voltage Switching

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ABSTRACT

DC-DC SEPIC Converter Design for Energy Harvesting Applications

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Master of Science Thesis

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With the design of ultra-low power wireless transceivers and the widespread use of battery-free applications, the participation of new autonomous agents in the constantly growing and developing world of Wireless Sensor Networks (WSN) and Internet of Things (IOT) is increasing exponentially. Energy harvesting applications, those efficient and operate in a wide input voltage range, increase the coverage and application areas of battery-free systems. For this reason, converters that are more efficient, consume less power and operate at larger input voltages are designed. Among these converters, structures providing bi-directional conversion, can provide further advantages in that bidirectional converters can also efficiently step down without excessive circuits, in addition to its boosting capability. Among them, SEPIC converters, which are becoming widespread in several areas, including renewable energy; are often preferred due to non-inverted output, non-excessive switch stress and considerably less input current ripple. Although, there are not enough studies in the literature in energy harvesting applications, SEPIC converters can offer more viable solutions.

In this thesis; it is aimed to investigate the effective use of partially integrated DC-DC SEPIC converters for very low voltage energy harvesting applications. For the start-up and control circuitry, a 7-stage ring oscillator and duty cycle control circuit which consists of transmission gate and inverters are utilized. In this context; using UMC 130nm technology; a robust energy harvesting system, capable of providing a constant 1V output with an input voltage range of 0.5V-1.6V is designed for thermoelectric and photovoltaic applications. Designed system offers an average output power of 2.7mW and a peak efficiency of 81%.

Keywords: SEPIC converter, energy harvesting, WSN, self-start-up

ÖZET

Enerji Hasatlama Uygulamaları için DA-DA SEPIC Dönüştürücü Tasarımı

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Elektronik ve Haberleşme Mühendisliği Anabilim Dalı

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Ultra düşük güçlü alıcı/vericilerin ve bataryasız çalışan uygulamaların yaygınlaşması ile birlikte, sürekli büyüyen ve gelişen Kablosuz Algılayıcı Ağları (WSN) ve Nesnelerin İnterneti (IOT) dünyasına yeni otonom ajanların katılımı da giderek artmaktadır. Verimli ve daha geniş giriş gerilimi aralığında çalışan enerji hasatlama uygulamaları ise bataryasız sistemlerin kapsayıcılığını ve uygulama alanlarını artırmaktadır. Bu nedenle daha verimli, daha az güç tüketen ve daha geniş giriş aralığında çalışabilen dönüştürücüler tasarlanmaktadır. Bu dönüştürücüler arasında çift yönlü dönüşüm sağlayan yapılar daha iyi avantajlar sağlayabilmektedir. Çünkü yükseltme yeteneklerinin yanı sıra çift yönlü dönüştürücüler fazladan devreye ihtiyaç olmadan verimli bir şekilde aşağı yönlü gerilim dönüşümü de yapabilmektedir. Bu dönüştürücüler arasında, yenilenebilir enerji başta olmak üzere birçok alanda kullanımı yaygınlaşan SEPIC dönüştürücüler; giriş akımında fazla dalgalanma yaratmaması, giriş gerilimi ile aynı polaritede çıkış gerilimi sağlaması, anahtarlama transistöründe aşırı strese neden olmaması vb. nedenlerle sıklıkla tercih edilmektedir. Ancak, literatürde

Enerji hasatlama uygulamalarında kullanımı konusunda yeteri kadar çalışma bulunmamasına rağmen, SEPIC dönüştürücüler bu alanda daha uygun çözümler sunabilir. Bu çalışmada; çok düşük gerilimli enerji hasatlama uygulamaları için tümleşik aktif elemanlı DA-DA SEPIC dönüştürücülerin etkili şekilde kullanılmasına yönelik kullanımının araştırılması hedeflenmiştir. Harekete geçme (start-up) ve kontrol amacıyla 7-katlı bir ring osilatör ve iletim geçidi (transmission gate) ile evirici içeren bir iş oranı kontrol devresi kullanılmıştır. Bu kapsamda; UMC 130nm teknolojisi kullanılarak, 0.5V-1.6V giriş gerilimi aralığında sabit 1V çıkış verebilen ve azami %81 verimlilikte ortalama 2.7mW çıkış gücü sunabilen DC-DC SEPIC dönüştürücü tasarımı yapılmıştır.

Anahtar Kelimeler: SEPIC dönüştürücü, enerji hasatlama, WSN, otonom çalışma

1
INTRODUCTION

The development and use of many technologies started for defense / military purposes and this phenomenon is widely accepted. One of these technologies, wireless sensors started to attract attention while the last century came to an end. In the simplest sense, wireless sensors can be described as small size and dispersed sensors which monitor different environmental data. To the best of our knowledge, wireless sensors for the first time were used by the United States Navy in a primitive concept for submarine detection at the beginning of the Cold War in 1950s. As a matter of fact, the sensors (hydrophones), located on the ocean floor, were connected to the data center located ashore via cables [1]. Then, first known studies on sensor network similar to today's technology started with the distributed sensor networks program at the US Defense Advanced Research Projects Agency (DARPA), around 1980 [2]. For the next four decades, with the development of MEMS technology and ultra-low power integrated circuits, the wireless sensor technology gradually improved. Over the years, wireless sensors have become a key technology for the near future.

It is a necessity to use wireless sensors in every system that complies with the concept of collecting and transmitting environmental data with small agents. Wireless sensors have a wide variety of applications, from deep seas to tropical forests, from the core of the earth to the farthest corner of space, from complex metropolises to remote villages, from autonomous machines to animal and human bodies. So how can we meet the power requirements of these so many sensors scattered all over the environment? Considering the energy needs of the wireless sensors, two common methods emerge; primary batteries and energy harvesting. Although primary batteries are a good solution for continuous and stable operation, they have several deficits which are size, limited storage, replacement

burdens, hazardous effects etc. These disadvantages result in limited working capacity of a wireless sensor. To prevent wireless sensors from being dependent on battery, energy harvesting enables nearly infinite operation without any human intervention.

The main function of energy harvesting is the conversion of environmental energy sources, which can be obtained in very low power and voltages by nature, into operating voltages with high efficiency. The voltages supplied by the harvesters which converts the ambient energy to the electrical energy may be higher or lower than the operating voltages of a wireless sensor. In this case, we may utilize three fundamental approaches: 1. stepping-up a higher voltage then stepping-down to operating voltage, 2. using bidirectional converters 3. applying switch capacitors. The first approach is much less efficient but it may present a very compact structure. The second approach, bidirectional converters are very useful when we consider efficiency with a wide input voltage range. But they may be expensive and bulky at the same time due to the discrete components like inductors and capacitors they consist of. And the third method does not maintain high efficiency for a wide range of ratios of input to output voltages. However, switching capacitor method, obviously has an important advantage of eliminating bulky inductors besides relatively high efficiency.

1.1 Literature Review

Considering energy harvesting applications for powering wireless sensors, there are various applications within a power span from a few $\boldsymbol{\mu W}$ to several $\boldsymbol{mW}$ in the literature [3]. Due to the nature of thermoelectric and photovoltaic energy harvesting, the harvested energy is available at millivolt levels by a majority. Especially micro thermoelectric generators and indoor photovoltaic cells are capable of delivering voltages around 1 volt (depends on harvester's size). Therefore, most of the power management circuits are designed as step-up structure.

Carlson et al. [4] proposed a inductor-based step-up DC-DC converter, fabricated in 130nm CMOS process, which was reported to supply a regulated 1V, from input

voltages ranging from 20mV to 250mV with approximately 50% efficiency for TEG harvesting. However, the converter's output capacitor must be pre-charged to approximately 650mV before the converter could kick over. Additionally, the input voltage span was not covering the voltages over 250mV.

Das et al. [5] proposed a single inductor-based step-up DC-DC converter, fabricated in 65nm CMOS process, with a peak efficiency of 75.9 %. The circuit was reported to boost a minimum 85mV input voltage to 550mV and 220mV input voltage to 1.3V output voltage after start-up operation completed. However, the output voltage was not fixed for different input voltages.

Yap et al. [6] presented a fully integrated power management system consisting of step-up converter, fabricated in 130nm CMOS process, which can convert 30mV voltage supplied from TEG module to a regulated 1.2V output enabling a PoR for start-up circuitry. Only a 30mV input voltage level was stated and the converting efficiency was not stated in the paper.

Machado et al. [7] presented an ultra-low-voltage step-up converter for thermoelectric energy harvesting that generates a 1V DC output from as low as 10mV input voltage. The proposed circuit, designed with zero-V_T 130nm, consisted of enhanced swing ring oscillator (ESRO) and Dickson charge pumps.

Nevertheless, there are many applications which implement bidirectional converting to exploit wide input voltage spans. Those of which have wide input voltage span and/or high converting efficiency at very low voltages are summarized below.

Chen et al. [8] proposed a single inductor dual-input dual output DC-DC converter for photovoltaic and piezoelectric energy harvesting, designed in 180nm process. The converter was reported to provide maximum %88.1 efficiency at 1.8V output with 60mA load current. In this study; there were two input options which were provided from piezoelectric and photovoltaic harvesters and the input voltages started from approximately 1V to approximately 3V. Therefore, the converting efficiency did not seem to severely suffer from voltage drops on the components.

Some researchers implemented switched capacitor conversion methods instead of inductor current transfer method. For instance; Saadat et al. [9] presented a fully integrated reconfigurable switched-capacitor converter that generates 1.2V output from a DC input voltage of 0.6V-2.4V or an AC input voltage with amplitude of 0.8 V - 2.6 V. The converter was implemented in a 250nm CMOS process and provides a peak 76% efficiency and 100μA maximum current. This type of conversion suffers from constant gain ratios dependent on switch numbers and has chaotic control mechanism.

Noghabaei et al. [10] proposed a fully integrated DC-DC converter, designed in 130nm process, which can convert 80mV of input DC level to 1V at a load resistance of 1MΩ with a conversion efficiency of about 24%. The converter consisted of fully integrated differential cross-coupled LC oscillator and LCP structures. Although the circuit had a capability of extremely low voltage levels, it did not have a fixed output voltage, the output voltage was changing due to input voltage and output load.

Damaschke [11] proposed a self-starting off the shelf DC-DC converter for wide-known bismuth-telluride thermoelectric module which can provide a stable output voltage of 5V for up to 131mW output load and 175Ω resistance with a 76% maximum efficiency. The harvester consisted of a micro transformer for start-up, a modified boost converter for the main circuit, a low voltage dual CMOS comparator enabled switching circuit and a MAX630 IC based supply circuit. Although the designed circuit could provide a reasonable efficiency as well as a high output power, it suffered from relatively narrow input voltage span and output voltage difference caused by input voltage variation.

Umaz [12] proposed a two-staged discrete converter, maximum power extraction stage (i.e. first stage) and a regulation stage (i.e. second stage), which can operate as low as 0.3V input voltage to step up 3.3V with maximum 140μW output power and maximum 24.69% efficiency for solar, TEG and MFC harvesting. The converter consisted of several IC as control circuitry and charge pumps. To reduce the minimum input voltage and increase the voltage span, the proposed converter was equipped with parallelly connected IC charge pumps. However, the converter

could only step-up a designated input voltage which was pre-boosted by charge pumps. Considering those studies above, the circuit structures for micro energy harvesting vary widely and many examples can be encountered similar to them. Nevertheless, to present a better understanding, the energy harvesting methods summarized in Table 1.1.

Table 1.1 Energy harvesting methods for TE and PV energies

Converting Method	- Step-Up - Step-Up/Down
Power Conditioning	- Switching Converters - Charge Pumps (Switching Capacitors)
Design Process	- Discrete - Integrated/Partially Integrated
Peak Efficiency	%10-%90
Output Power Span	1 μW-100mW

When we think of bidirectional DC-DC converters regarding thermoelectric and photovoltaic energy harvesting, the most popular one is buck-boost converter. But SEPIC converters are gaining much more fame recently, especially in the area of renewable energy conversion. SEPIC converters, which may seem disadvantageous at first glance due to having more circuit elements than the buck-boost converter, are also frequently used for photovoltaic, thermoelectric and mechanical energy conversion systems at low, medium and high voltage due to the other advantages they offer [13]. In the literature, SEPIC converters are studied widely in several areas, including renewable energy, power factor correction, electric vehicles, led lighting, street lighting, water pumping and high power/voltage applications [13], however there are quite a few applications for micro energy harvesting.

Grace et al. [14] presented the performance evaluation of different rectifiers for piezoelectric energy harvesting applications. In this specific comparison, SEPIC was used to rectify and regulate 3.2V (peak) AC input voltage to 2.68V with a 97.6% efficiency. In this study, efficiency did not suffer from voltage drops on the

components, but the circuitry only step-down a specific input voltage to a desired output voltage.

Schwartz [15] presented a maximum power point tracking system architecture to maintain an optimal power extraction from a TEG (Tellurex G1-40-0322). To demonstrate the functionality of this MPPT architecture, a SEPIC converter which had a maximum 69% of efficiency was implemented. As stated in the experimental results; the MPPT circuit was increasing the efficiency between 0.7V-1V input voltages considerably, but still output voltage was not fixed for input voltage variations.

Wu et al. [16] proposed a wearable energy harvester based on SEPIC converter for photovoltaic energy harvesting. The fabricated harvester had an overall efficiency of 66.2% at 25mA load current and 2.5V output voltage when a solar input voltage of 3.05V had been supplied. It was a unique DC-DC SEPIC converter example reported for wearable electronics; however, the input voltage variation was not considered as a design parameter.

Ullah et al. [17] proposed an analog controlled DC-DC SEPIC converter for solar powered WSNs. The converter was reported to convert 2V-17.1V input voltage range to regulated 3.3V with a maximum efficiency of 99%. The efficiency at the 2V input voltage level was reported 94.7 % with 24.6mW output power and 7.5mA current for 500Ω resistive load. The proposed circuit had a significant efficiency and wide input span, but it did not cover the sub-1V area which is challenging for efficiency considerations.

Bagci et al. [18] implemented SEPIC converter as the parallel differential power processing (DPP) converter used in a PV implemented bag system. The experimental results were reported that efficiency of the SEPIC alone showed a maximum 63.5%, while the highest DPP system efficiency reached 78.4%, which was an improvement of 14.9%. The prototype consisted of two 0.3W cells and two 1.5W cells to achieve up to 3.6W of power, with the DPP converters sewn inside the bag. The SEPIC converter was used only to step-up the 4.1V and 4.8V input voltages to 5V separately.

Poluthai et al. [19] studied on a PI controlled SEPIC converter for a TEG module which was designed to power portable energy storage and mobile devices. The converter reported to convert 15V-25V input voltage to regulated 12V output voltage at the resistive range of 80Ω-120 Ω. The flexibility and robustness of the system was not obvious, because a continuous input voltage variation was not applied to the converter.

As a different energy source; human activity which provides an alternating voltage was used by Wang et al. [20]. They proposed a SEPIC converter based energy harvesting interface circuit for backpack energy harvesting system which was reported by Rome et al.[21]. The output of the backpack mechanic generator was rectified by Schottky-diode rectifier, then connected to SEPIC converter for regulation. The overall efficiency was 82.2% (battery charging) while input power was reported to be 20.32W. Nevertheless, there were several integrated circuits for digital control and that caused a very high form factor.

To present a better understanding, SEPIC studies are summarized in Table 1.2. In addition to the above-mentioned scientific studies, there are many applied integrated SEPIC solutions for different applications such as automotive, industrial supplies, powering portable products etc. As seen in Table 1.2, SEPIC converter design operating at powers below 25mw is not available as far as we know.

Table 1.2 SEPIC converter applications for energy harvesting

Application Types	PV, TE, PE Energy Harvesting Renewable Energy Conversion (Solar) MPPT Circuits
Circuit Design Type	Discrete Design
Peak Efficiency	Varies between %63.5 and %99
Output Power Span	25mW - 50W
Input Voltage Span	2 V-25 V
Input Current Types	Both AC and DC

As proved in [22], the SEPIC converter can produce good results considering efficiency, wide input voltage range and high static voltage gain. The SEPIC converter is also preferred due to its advantages which are non-inverted output, non-excessive switch stress and considerably less input current ripple. Especially since the problems such as the control difficulty of the switching transistor and the reverse polarity output voltage caused by the widely used Buck-Boost converter are not seen in the SEPIC converter, it is suitable for use in many areas. In order to eliminate the disadvantage of having more losses due to additional components of SEPIC, two inductors can be coupled. At the same time the couple inductors will result in a more or less an increase in efficiency as well.

1.2 Objective of the Thesis

Due to advantages such as providing bidirectional conversion, non-inverted output, non-excessive switch stress and considerably less input current ripple, SEPIC converter is widely used recently. Along with the aforementioned benefits, the use of this converter structure in energy harvesting applications is gradually increasing, however there is a gap in the literature regarding its use at very low voltages. Micro-scale energy harvesting transducers, by their nature, often generate voltages around 1V or several hundred mV. Implementing properly, SEPIC converters, with the ability of bi-directional converting, can present remarkable results for such low voltages.

In this thesis, it is aimed to investigate the effective use of partially integrated DC-DC SEPIC converters for very low voltage energy harvesting applications. Therefore, with an inverter based 7-stage ring oscillator and duty cycle control circuitry designed for start-up and control, a stand-alone energy harvesting system without the need for a complex control circuit is presented.

1.3 Hypothesis

Harvest and Use battery-less systems are preferred generally for their relatively unlimited lifetime. When there is enough energy, they take action and start

operating. Therefore, the converters used in these systems are required to be capable of operating quite efficiently and accept wide input voltage range. Bidirectional converters can meet these requirements without the need for additional circuits. As one of the bidirectional converters, SEPIC converter is highly preferred recently due to the advantages it provides. It is studied and applied generally for the areas including renewable energy, EV, Plug-in EV, street lighting, led lighting, PFC etc. However, there is not enough study of SEPIC converters in energy harvesting applications. Exploiting the advantages of it, DC-DC SEPIC converters can be efficiently utilized for “Harvest and Use” energy harvesting applications as well.

2
BATTERY-LESS OPERATION VIA ENERGY HARVESTING

Our unique world, which has recently been surrounded by trillions of sensors and tiny agents, is now facing with the environmental impact of ever-growing battery waste. According to the World Economic Forum insight report; the global battery demand will be 14 times bigger than today [23]. Based on this information we can reach a conclusion that if applicable, “everything that can be electrified will be electrified” [24]. Undoubtedly, such a large demand can have many negative consequences. Of course, the most important of these negative consequences is environmental damage. In addition to environmental pollution, the batteries have many disadvantageous features which are: constraining form factor, replacement costs, replacement or recharging burdens, restricted lifespan etc.

To deal with battery waste without interfering with the fulfillment of energy demand, researchers have been focused on battery-free solutions. Instead of using stored energy packs, researchers have suggested operating our devices using very low energy resources available in our environment surrounding us. We can gather or harvest these energy sources to convert electrical energy by means of proper harvesters. Here we call this energy obtaining phenomena as “Energy Harvesting” or “Energy Scavenging”.

Advances in transducer technology, which converts other energies into electrical energy, enabled us to get more energy per unit area. In addition, increasing reliability of transducers to provide more consistent and sustainable energy has made energy harvesting more common and used in many areas. Just as the power available from transducers has been increasing, the power needed to operate electronic circuits are getting lesser. Power consumption of the electronic devices has been a major concern for designers and researchers. This concern motivated

them to design small and smart circuits which consume less power resulting in devices that can be powered easily via energy harvesting. On the other hand, every tiny device such as wireless sensors are going to be connected to the internet like our smartphones, computers and watches. Therefore, energy dependence will be more and more important for future designs. As a result of all these developments, we can say that energy harvesting, which can significantly eliminate energy dependence, will be in all areas of our lives in the future.

Energy harvesting can be enabled for assisting the existing battery or it may be implemented as a sole power source for the application. From the perspective of reducing battery pollution, a limited improvement can be made by implementing batteries. Yet, our ultimate goal in this study is to provide battery-free operation. The very first step in bringing into being the energy harvesting is to determine the power consumption of the device or application. Here, we should also determine the working principle of the application. Working principle provides us the information of intermittent operation and quiescence power levels which are important considering scarce energies.

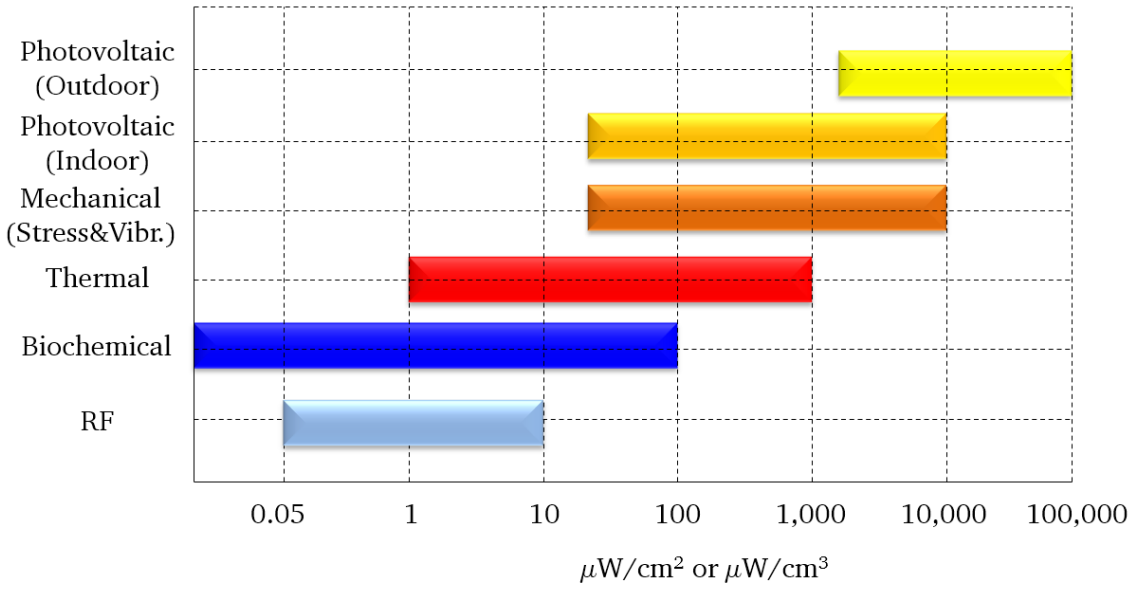


Figure 2.1 Environmental energy sources and densities [25]

Environmental energies that we can harvest are diverse and have different densities, as seen Figure 2.1. It is important to choose the appropriate energy source according to the device to be used. Furthermore, to improve the energy stability of an energy harvesting powered device, a hybrid energy solution should be taken into consideration.

Assuming a wireless sensor to be powered via energy harvesting, the complementary energy sources can be chosen to ensure continuous operation. For instance; photovoltaic energy is a suitable source for illuminated areas, however the operation is restricted by the end of the illumination. To overcome this issue, thermal energy as a secondary power source can be implemented. After deciding the energy source(s), we should determine the harvester sizing as a second step. Harvester size can increase the form factor dramatically. Considering photovoltaic and thermal energies; a $50X50\ mm^2$ photovoltaic energy harvester (solar cell) can provide minimum 1.25mW and maximum 25mW output power, while a thermal energy transducer (Peltier etc.) should be expected to provide minimum 25μW and maximum 25mW output power.

2.1 Ambient Energy Sources

Ambient energy sources known as solar, thermal, mechanical, biochemical, and RF energies have different advantages, disadvantages, restrictions, abundance or attributes. The most popular and widely known among them is, of course, solar energy. Therefore, applications that work with the photovoltaic phenomenon are more common. The widespread use of mobile applications carried by people has also spread the use of thermal energy and mechanical energy originating from the human body. Especially in the urban areas, the abundance of RF radiance increases the use of RF energy. As stated above, all energies must be held in its unique way to exploit them properly. Since photovoltaic and thermal energies are aimed in this study, detailed information about these energy sources is presented below.

2.1.1 Photovoltaic Energy

Photovoltaic energy is the most abundant and popular energy source among the ambient energy sources. The energy is generated by the phenomenon known as photovoltaic effect demonstrated in Figure 2.2 [26]. The energy radiated by the energy source which can be artificial or solar, is absorbed by the transducer and reaches to electrons. The excessive energy creates an electric potential at the boundary of n- and p-type joint area. This phenomenon is named as the photovoltaic effect.

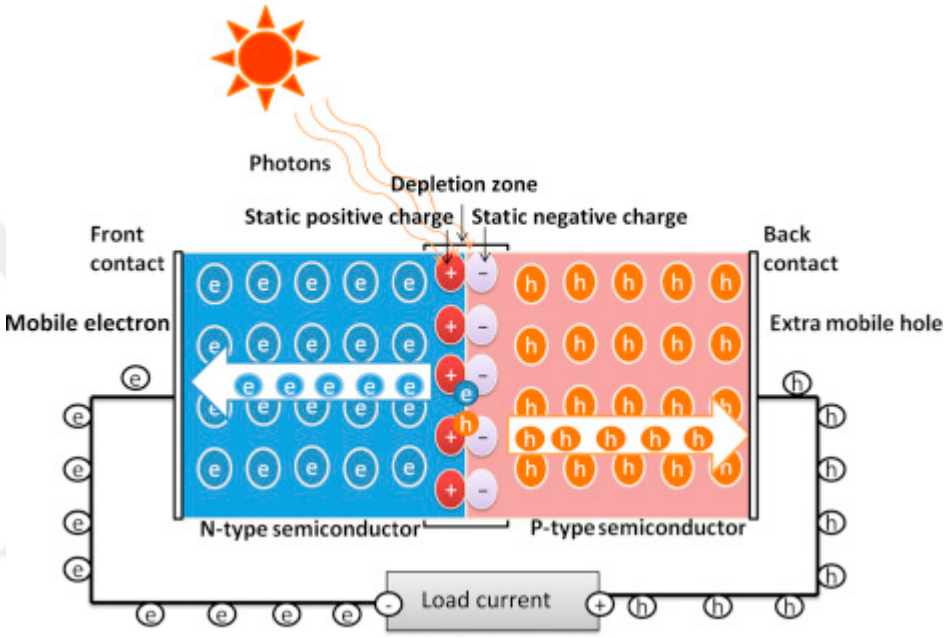


Figure 2.2 Photovoltaic effect [26]

Although there may be degradation in efficiency over time, the most important parameter for photovoltaic cells is cell efficiency. From the late 70's till now, a single cell has come a long way regarding efficiency considerations. With the development of multijunction and concentrator cell technology, the efficiency has reached almost 50 % [27] for outdoor.

Photovoltaic energy has some advantages and disadvantages. It never harms when it operates, clean, does not emit any toxicant, does not need maintenance, usable wherever the photons reach. The voltage generated at the output of a solar cell does not change suddenly, unless blocked. Due to its DC characteristic voltage, additional circuits or components are not needed to rectify. The main

disadvantage of photovoltaic energy is that it cannot generate energy in night time or off office hours.

The potential use of solar energy harvesting applications is vast, due to its viable advantages. From IOT to WSN, street lighting to satellite power, wristwatches to calculators, off-shore oil rigs to lighthouses, water pumping for agriculture to cooling plants, there are tons of applications of solar energy harvesting which scales from μW to kilowatts.

2.1.2 Thermoelectric Energy

Similar to photovoltaic energy thermoelectric energy has several advantages which make it viable for many applications. Thermoelectric energy harvesting is based on the electric generation of thermoelectric generator (TEG) that operates via *Seebeck Effect* which occurs when a temperature gradient provides a voltage generation at the conductors [28].

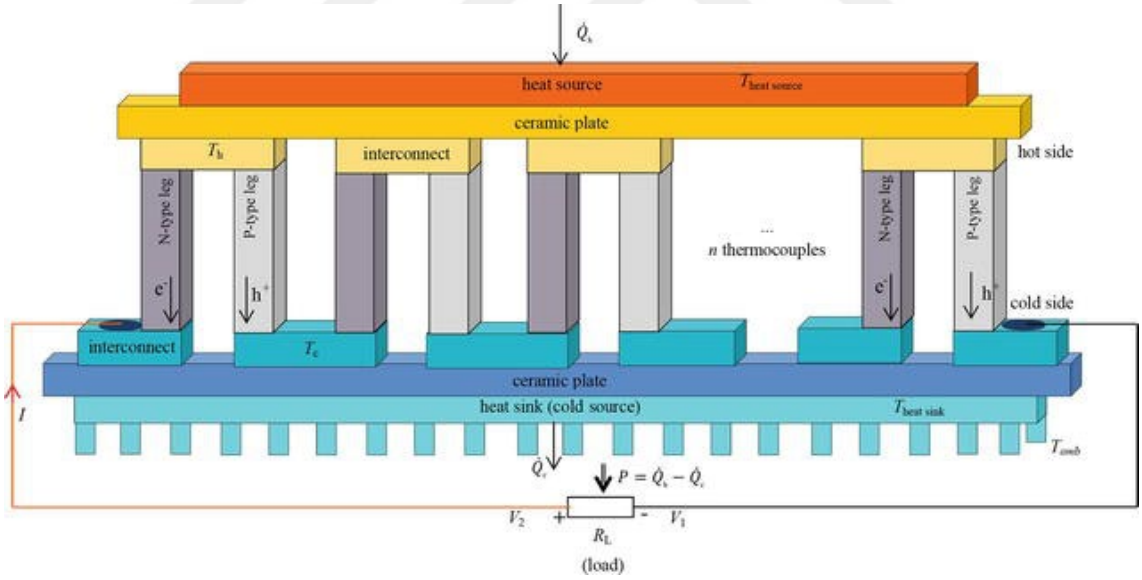


Figure 2.3 Thermoelectric Generator (TEG) with "n" thermocouples [28]

Unlike photovoltaic ones, thermoelectric transducers have a limited efficiency around 5-15%. These transducers can operate anywhere a temperature difference is available. However, its limited efficiency restricts the extensive utilization. In the future, the new thermoelectric material technology may allow more efficiency levels.

The most important advantage of thermoelectric energy is that it needs relatively no maintenance. The other advantages are those; it is easy to integrate with the existing hardware and very affordable when compared with other transducers. The most disadvantageous attribute is the low thermal efficiency.

From low power applications to waste heat recovery applications, the power range of thermoelectric energy spans from tens of μW to kilowatts. Especially for the micropower applications, the human body heat is widely used for thermoelectric conversion. Thermo-powered wristwatches are the most known micro application widely used. Besides, there are biomedical, WSN, space and residential applications of thermoelectricity [28].

3
VERY LOW VOLTAGE CONVERTER DESIGN

3.1 Main Converter Design

Due to the very low voltage characteristics of energy harvesting applications, converters are expected to be able to work stable and at high efficiency values at the lowest possible voltages. Harvesting topologies also differ when the voltage values that micro energy sources can produce from a few 100 millivolts to several volts need to be increased or decreased to the operating voltage.

Although it increases losses and costs due to having an extra coil and capacity compared to the DC-DC Buck-Boost converter, The SEPIC converter can stand out as a highly effective converter for low-energy harvesting application due to the fact that the input voltage and the output voltage are in the same polarity, it creates lower input voltage ripple and is easier to control. Transducer's output voltage shall be converted to 1V as feed in the UMC 130nm process which is frequently used in this technology. In this context, the lowest input voltage was determined for 1V fixed output voltage and input voltage was optimized according to the operating range. Designated SEPIC design parameters are shown in Table 3.1.

Table 3.1 Low voltage DC-DC SEPIC converter design parameters

Parameter	**Value**
Output Voltage	1 V
Minimum Input Voltage	0.15 V
Maximum Input Voltage	1.6 V
Maximum Output Voltage Ripple	±0.05V
Design Process	UMC 130nm

Considering that the converter is in steady state and the voltage and current values are periodic, the input-output voltage relationship, including the switching loss will be:

$$V_o = V_s\left(\frac{D}{1-D}\right) - V_D \tag{3.1}$$

Although the schottky diode provides a lower forward voltage drop (≈200mV), it causes sudden voltage spikes due to its very rapid current change. These sudden voltage spikes cause both more stress on the circuit elements and decrease in efficiency. In addition, in order to reduce the number of non-fractured elements, a diode-connected MOSFET that can present a smoother current-voltage curve was used in the converter design. When the maximum voltage drop on the diode connected MOSFET is V_D=240 mV and the maximum applicable work rate is D=0.9, the minimum input voltage for 1V output voltage can be calculated as:

$$1V + 0.23V = V_s\left(\frac{0.9}{1-0.9}\right) \Rightarrow V_s = 0.14V$$

Assume that frequency and load of the DA-DA SEPIC converter are constant, output voltage ripple is highly dependent on the output capacitor (3.2.). Less fluctuation at the converter output is important for the health of the load to be connected. For this reason, the capacity calculation that will allow a voltage fluctuation of at most 5% at the output is made as follows.

$$\Delta V_o = \frac{V_o^2}{RC_{out}f(V_i + V_o)} \tag{3.2}$$

From equation (3.2), output voltage ripple can be calculated as:

$$C_{out} = \frac{V_o^2}{R\Delta V_o f(V_i + V_o)} = 0.45\mu F$$

The converter is designed to work in both CCM and DCM modes for different input voltages in order to keep the input voltage range as wide as possible. L1 and L2 inductor currents are decisive for the both operating modes. That is, if the inductor currents always show a value and do not drop to zero, then the SEPIC converter is operating in CCM mode. It is the opposite for DCM mode as well. Comparison of the inductor currents and load current which is depicted in Figure 3.2 can present a better understanding for CCM and DCM discrimination. Boundaries between the operation modes can be determined via the lowest point of the inductor currents I_{LV1} and I_{LV2}.

For the $I_{LV1} + I_{LV2} > I_{out}$ condition SEPIC converter operates in Complete Inductor Supply Mode (CISM)-CCM mode described in Figure 3.2.(a). In this mode; the diode connected NMOS is conducting and output capacitor is recharging. When $I_{LV1} + I_{LV2} < I_{out}$, converter operates in Incomplete Inductor Supply Mode (IISM)-CCM mode where the diode connected NMOS is conducting and the output capacitor is discharging. For the condition $I_{LV1} + I_{LV2} = I_{out}$, the converter operates in IISM-DCM mode in which the load supplied only by output capacitor. There are two critical inductance values for the SEPIC converter operating modes. The first one describes the critical inductance value $L_{Ke,}$ between CISM and IISM determined by the equation (3.3) [29]. For $L_e > L_{Ke}$, the converter is in CISM mode and for $L_e < L_{Ce}$ the converter operates in IISM mode.

$$L_{Ke} = \frac{R_L}{2f} \frac{V_i^2}{V_o(V_o + V_i)} \tag{3.3}$$

The critical inductance value between CCM and DCM can be obtained by the equation (3.4). For $L_e > L_{Ce}$, the converter is in CCM mode and for $L_e < L_{Ce}$ the converter operates in DCM mode.

$$L_{Ce} = \frac{R_L}{2f} \frac{V_i^2}{(V_o + V_i)^2} \tag{3.4}$$

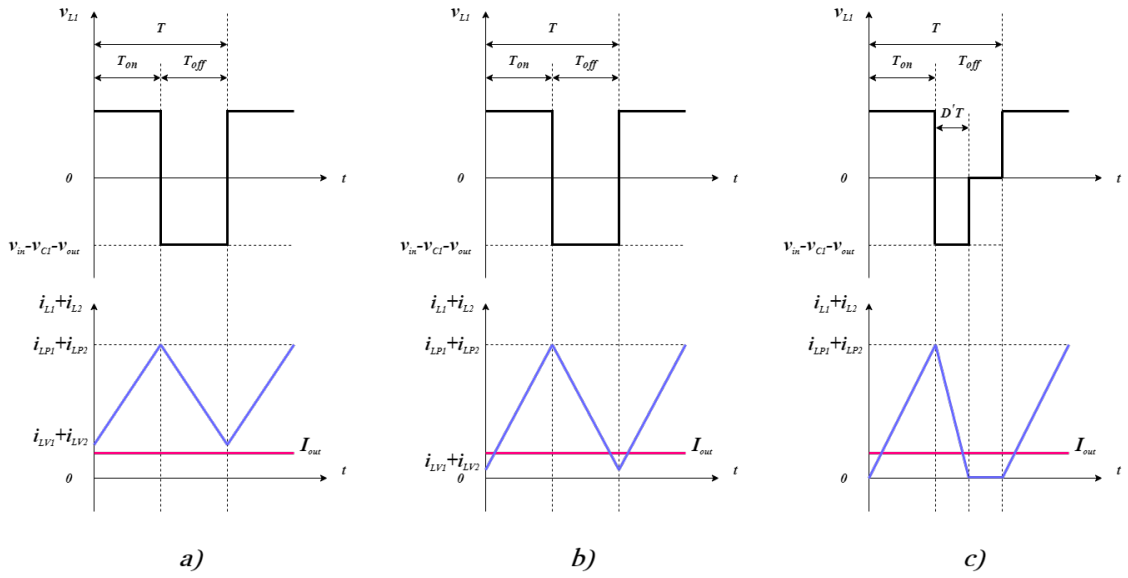


Figure 3.1 Different operating modes of SEPIC; a) CISM-CCM, b) IISM-CCM and c) IISM-DCM [29]

The other crucial parameter has to be taken into consideration is the switch peak current (SPC) which directly affects the stress and efficiency. A minimum SPC is desired to get a maximum efficiency and prolong the lifetime of the components. When the switching transistor is on, SPC can be calculated as the sum of peak inductor currents [29] as stated in equation (3.5).

$$I_{SP} = I_{LP1} + I_{LP2} \tag{3.5}$$

SPC in CCM mode is determined by as follows:

$$I_{SP}^{CCM} = \frac{V_{out}(V_{in} + V_{out})}{R_L V_{in}} + \frac{V_{out} V_{in}}{2 f L_e (V_{in} + V_{out})} \tag{3.6}$$

Likewise, SPC in DCM mode is calculated as below:

$$I_{SP}^{CCM} = V_{out} \sqrt{\frac{2}{R_L f L_e}} \tag{3.7}$$

Considering equations (3.6) and (3.7), SPC level is reversely dependent on inductor and resistance values. Therefore, for certain load conditions, the inductor

values should be high enough to restrict the excessive currents in the switching transistor.

According to Table 3.1 and equations above, SEPIC converter elements are determined as; L1 // L2 = L_e = 300μH, C1 = 47nF, C2 = 0.45μF. Here, L_e stands for the equivalent inductance value of the parallel inductors. As for the switching transistor and output diode, UMC 0.13um Logic 1P8M High Speed Enhancement N-MOSFET is used. The SEPIC converter circuit diagram designed based on the above parameters is presented in Figure 3.2. Transistors used in the converter circuit are the type of BPW-NMOS. Switching transistor has a dimension of 10μm width, 0.12μm length, 10 fingers and 5 multipliers. On the other hand, the diode connected output transistor is much larger and has the dimension of 100μm width, 0.84μm length, 10 fingers and 10 multipliers. The transistor sizing is explained in Appendix-A in detail.

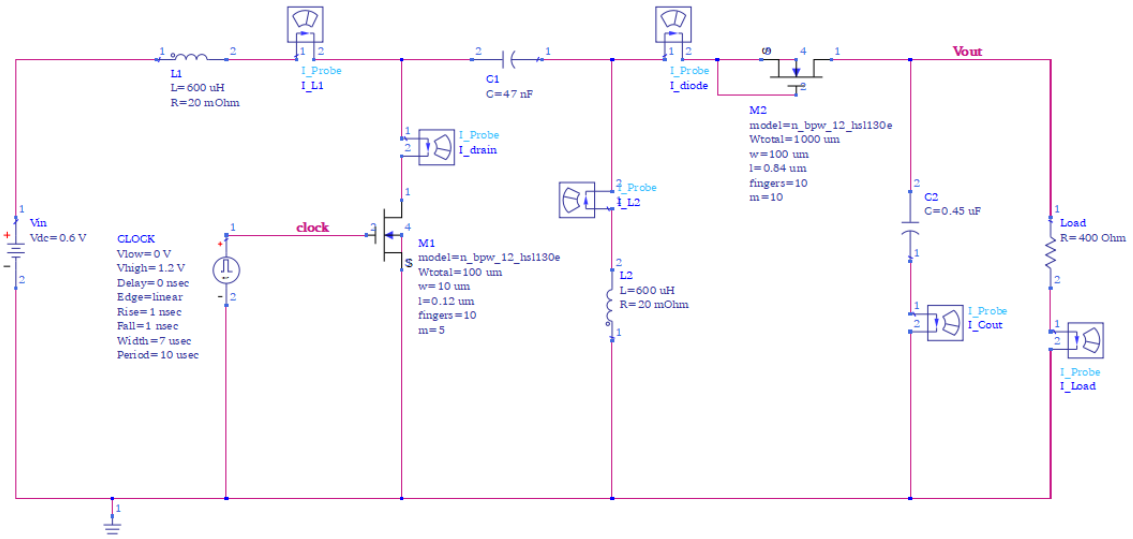


Figure 3.2 Low voltage DC-DC SEPIC converter circuit

3.2 Control Circuitry

Switching the transistor at low frequencies ensures that losses are significantly reduced. Therefore, N-Channel MOSFET transistor of the main converter is aimed to be switched at around 100 KHz. In order to keep the oscillator that will generate the switching signal around this frequency, the oscillator design should be designed and controlled properly.

A voltage controlled 7-stage ring oscillator and adjustable duty cycle control circuit [30] has been implemented for control circuitry. Operation principle can be described by 4 fundamental steps: *i)* a square wave is generated by the ring oscillator, *ii)* after refining the oscillator output the signal is converted to a triangle wave, *iii)* triangle wave then merged with the reference converter output voltage and turns into square wave, *iv)* finally the signal refined again and applied to switching transistor of DC-DC SEPIC converter. Control operation is described in the block diagram in Figure 3.3.

To enable lower input voltages to be boosted, the input voltage and output voltage being fed together into the control circuit. The input voltage is connected to the control circuit with a PMOS which is biased by output voltage. Likewise, the output voltage is also fed to the control circuit with an NMOS transistor. This type of connection makes the system more robust for a wide input voltage span.

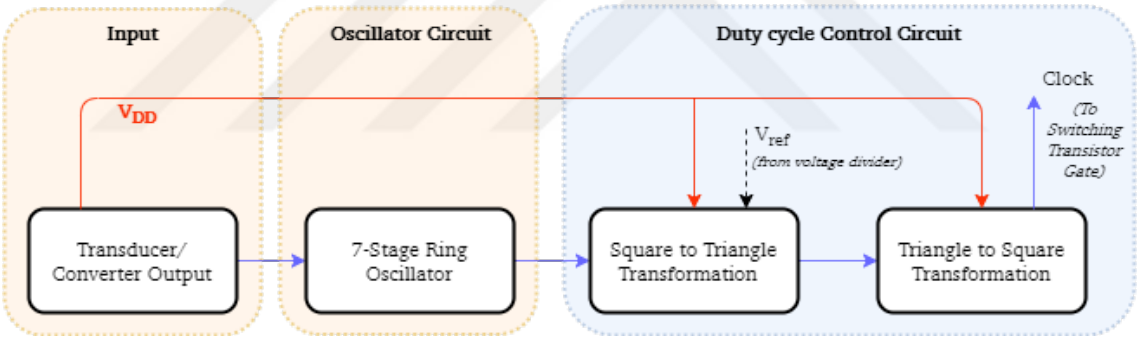


Figure 3.3 Control operation block diagram

3.2.1 Ring Oscillator

To get the converter to take on, a single-ended 7-stage ring oscillator has been implemented in this study. The ring oscillator generates quite sharp square wave signal which is going to be used as triggering gate voltage. Delay of each inverter and odd numbers of the whole oscillator result in the oscillation frequency.

$$f_o = \frac{1}{2n\tau_{inv}} \tag{3.8}$$

Where n is the odd number of the inverter count and τ_{inv} is the single inverter's stage delay which consists of the sum of rise and fall time ($\tau_{inv(HL)}$, $\tau_{inv(\mathrm{LH})}$). Determining the exact frequency of a ring oscillator can be challenging, although there are several common expressions in the literature. Michal [31] has proposed a much sensitive approach which is based on the inverter delay equation (3.9).

$$\tau_p = \frac{2C_{ox}L^2(k+1)(V_{DD}-2V_{TH})}{(V_{DD}-V_T)^2}\left(\frac{1}{k.K_{pp}}+\frac{1}{K_{pn}}\right) \qquad (3.9)$$

Where, C_{ox} is the oxide capacitance, L the transistor length, k the scaling ratio between PMOS and NMOS channel width, V_{DD} the supply voltage and $K_{pn} = \mu_n C_{ox}$, $K_{pp} = \mu_p C_{ox}$.

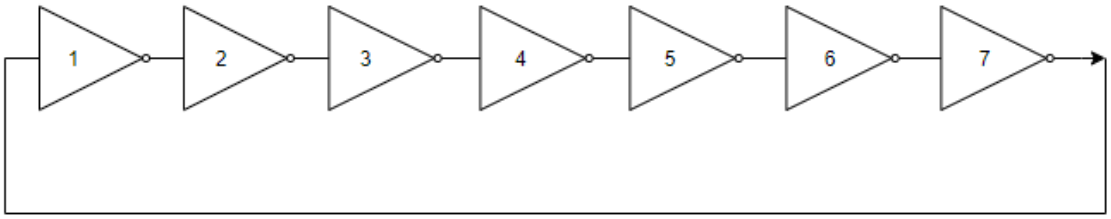


Figure 3.4 Cascaded inverter ring oscillator (7-Stage)

Given that, $V_{DD} = 0.8V$ which is going to be attained directly from both the transducer's and main converter's output node simultaneously, $t_{ox} = 27.3\,\text{Å}$, $\mu_n = 415.5cm^2/V.s$, $\mu_p = 120.5cm^2/V.s$, $k = 1$ (W/L scaling ratio) and $V_{TH} = 0.234V$ the calculated frequency of ring oscillator will be 73KHz approximately. Detailed design calculations can be found in Appendix-B.

Power dissipation of a ring oscillator grows out of two reasons. One of them is the cross-conduction loss which caused when the inverter input voltage is close to $V_{DD}/2$. In this transition time, both NMOS and PMOS conduct simultaneously. The other factor is the capacitive loss, which caused by the charging and discharging of the inverter's capacitances [32].

$$P = n\frac{CV_{DD}^2}{\tau_{inv}} \tag{3.10}$$

Where C is the total capacitance on the output node and n is the total number of stages. Although the simple equation given above allows us to gain a certain point of view, it is not sensitive enough to determine the exact oscillating frequency. Therefore, another much more sensitive model, which is given in equation (3.11) is applied for calculations [31]. Note that, the cross-conduction losses are neglected in this model.

$$P = \frac{W}{L}\frac{V_{DD}^2(V_{DD}-V_T)^2}{2(V_{DD}-2V_{TH})\left(\frac{1}{k.K_{pp}}+\frac{1}{K_{pn}}\right)} \tag{3.11}$$

As seen from the equation above, the lower the W/L ratio, the lower power consumption is. Thus, the oscillator has been designed the edge of its W/L limitations. Longer transistor length also increases the inverter delay and causes low oscillating frequency which reduces the switching losses on the DC-DC converter side. For the designed 7-stage ring oscillator depicted in Figure 3.4, ignoring cross-conduction losses, power consumption is at nanowatt level dependent on input voltage.

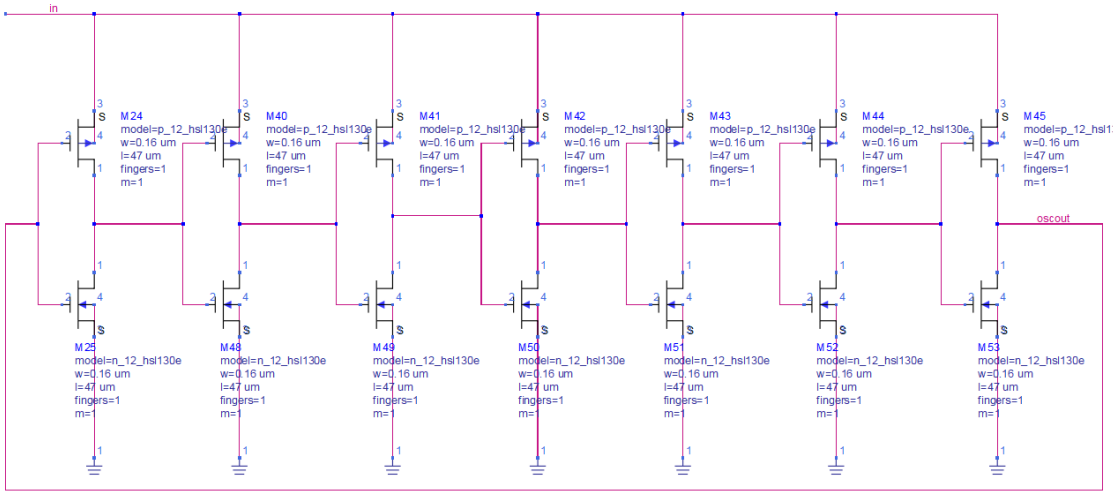


Figure 3.5 7-Stage ring oscillator designed in 130nm process

3.2.2 Duty Cycle Control Circuitry

Duty cycle control circuit consists of a transmission gate, a pair of parallel connected two inverters which act like an inverter and refinement inverters.

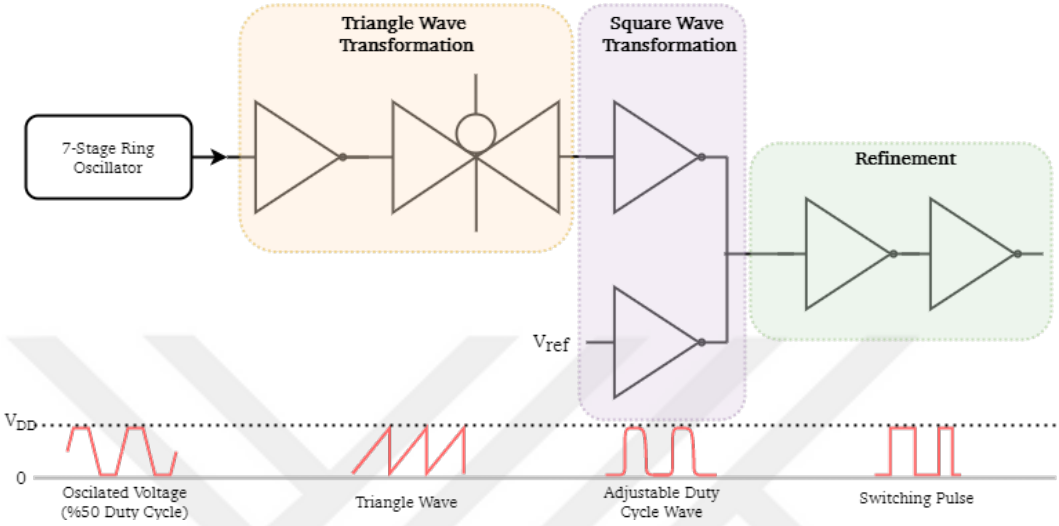


Figure 3.6 Duty cycle control operation

The transmission gate in the triangle wave transformation circuit seen in Figure 3.6, acts as a very large resistor which can suppress the charging and discharging of the previous inverter to get the signal nearly linear. By implementing this transmission gate, the square wave coming from the previous inverter always turns into a triangle wave whatever the frequency is.

After acquiring the triangle wave, the signal is applied to an inverter which is parallel with another inverter. At that time, a reference voltage (V_{ref}) acquired from the main converter's output node with a voltage divider, is applied to the other parallel inverter. Reference voltage (V_{ref}) can control the ON resistances of parallel inverter transistors so the duty cycle can be controlled as well. This operation is called "Triangle-wave to Square-wave Transformation" because the generated output signal of the parallel inverters is nearly square.

4
SIMULATIONS AND EXPERIMENTAL RESULTS

DC-DC SEPIC Converter and control circuitry is designed with UMC 130nm CMOS Technology and simulations are conducted with Advanced Design System (Keysight). The system has discrete components such as inductors and capacitors which makes the system partially-integrated. Whole system architecture is depicted in Figure 4.1 which blue colored section is main converter, magenta colored one is ring oscillator and green colored stage is duty cycle control circuitry. To give a detailed explanation, simulations are divided into two sections. First section consists of individual simulation and analyses of the main converter, ring oscillator and duty cycle control circuitry. The second section explains the harvesting system end to end simulations.

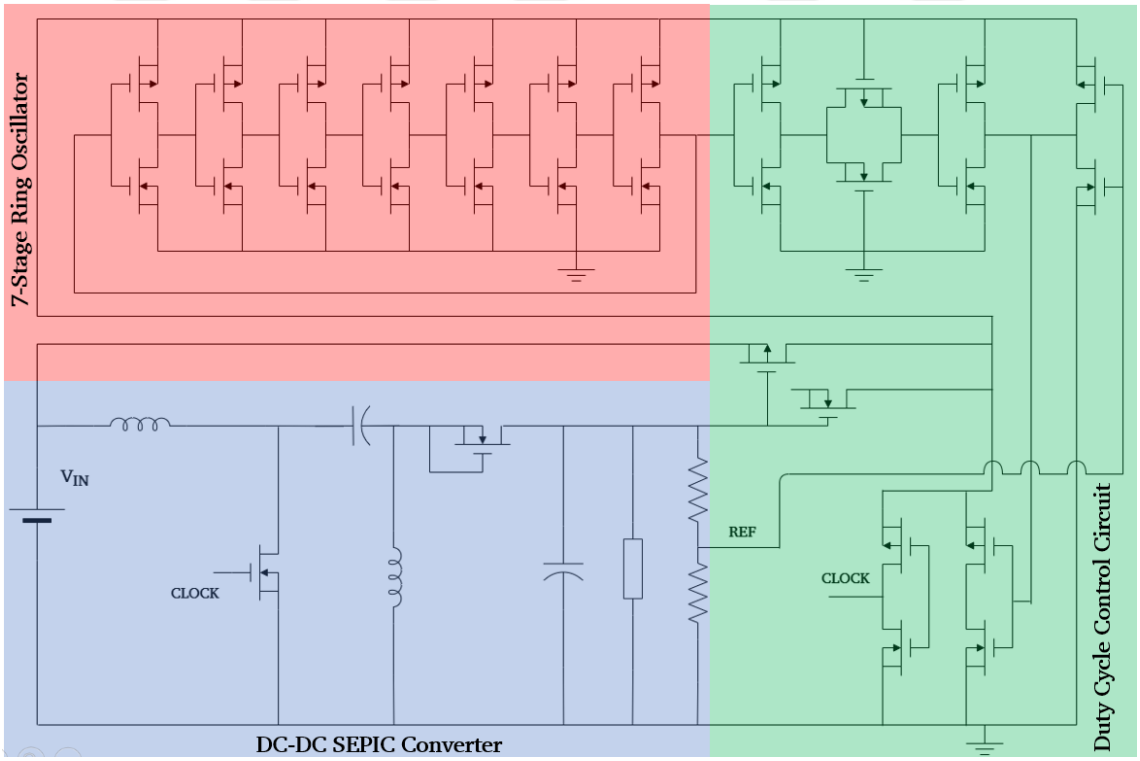


Figure 4.1 System architecture

4.1 Main Converter Simulations

DC-DC SEPIC converter which works as a main converter has a quite wide input voltage span to boost and buck convert to 1V. Solely for the main converter, it has been observed that it converts the wide input voltage between 0.15V and 1.6V to 1V output voltage with 81% peak efficiency.

4.1.1 Main Converter Voltage and Current Waveforms

As a result of the simulations executed for the DC-DC SEPIC converter, the voltage and current waveforms are demonstrated in Figure 4.2. Blue line shows the primary inductor current which is connected directly to input, green line shows the gate signal which is supplied virtually for this simulation and red line shows the regulated output signal.

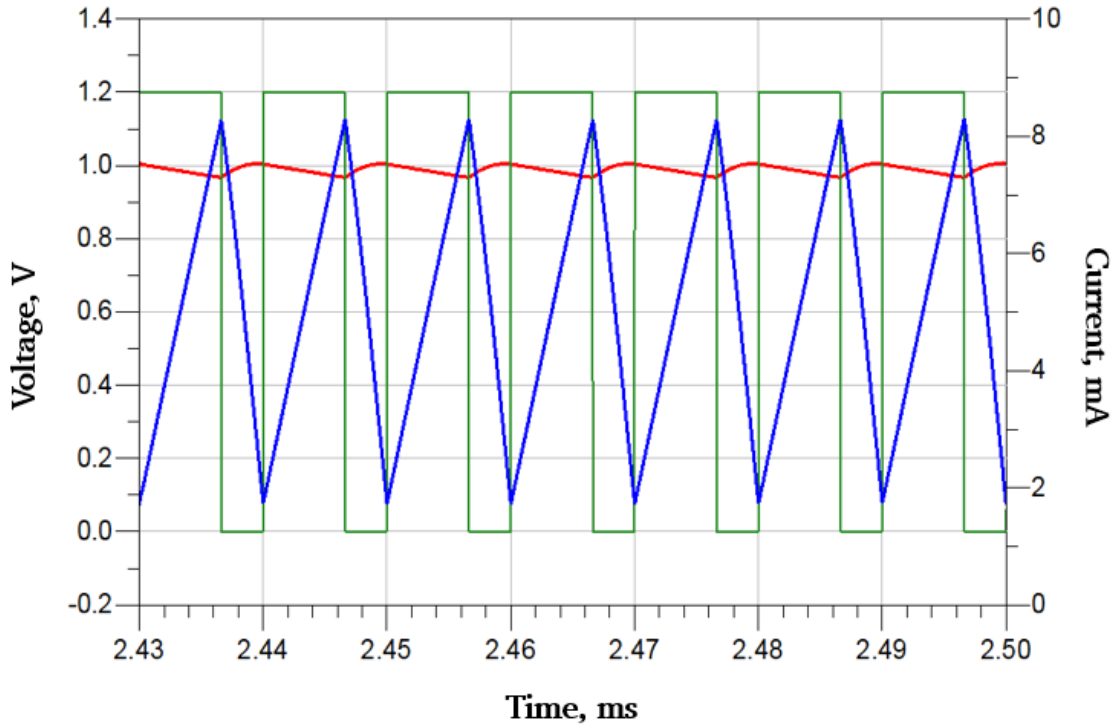


Figure 4.2 Current and voltage waveforms of main converter

With the virtual gate voltage which is 100 Khz and oscillates between zero V and 1.2V, the SEPIC converter operates both in CCM (Continuous Conduction Mode)

and DCM (Discontinuous Conduction Mode) modes. Between 0.15 and 0.6V input voltages converter operates in CCM mode and between 0.7 and 1.6V input voltages converter operates in DCM mode as well. The inductor current waveforms in CCM and DCM modes are displayed in Figure 4.3. The blue line shows the CCM mode when input voltage is 0.4V and the red line shows the DCM mode operation when the input voltage is 1.2V.

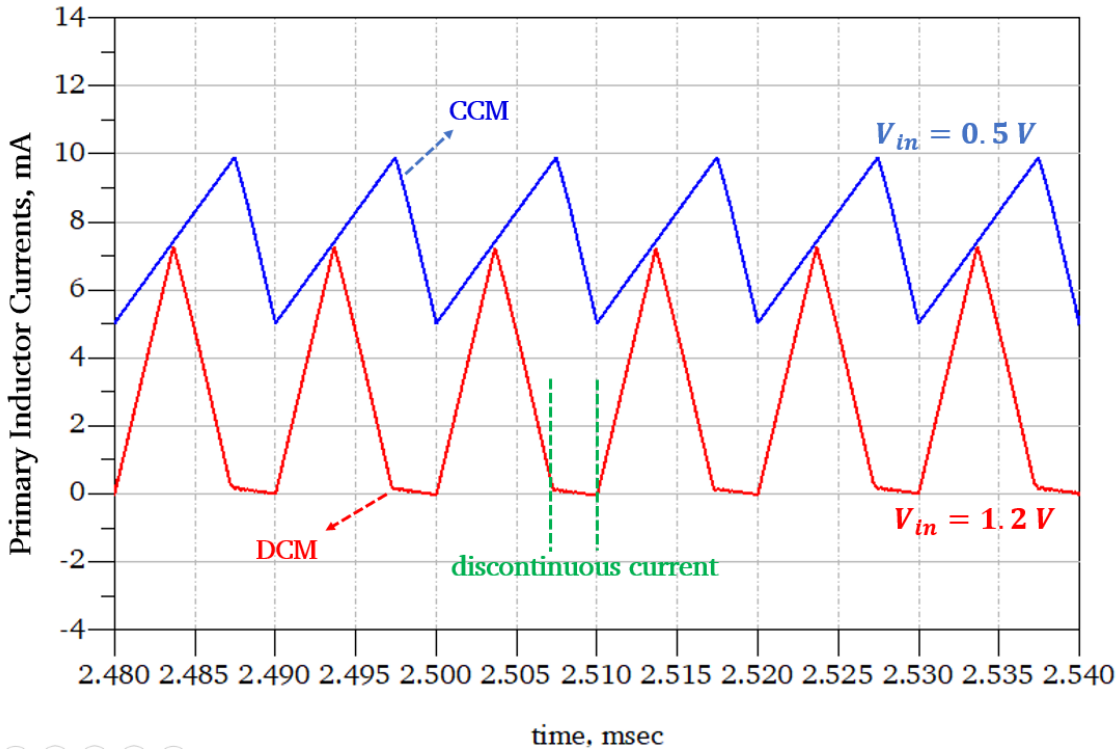


Figure 4.3 CCM and DCM operation for 0.4V and 1.2V input voltages

Switching signal rise / fall time is chosen high enough not to disturb the converter switching synchronization, but low enough not to create excessive stress on the circuit elements. Assume that, the gate signal has a 1 nanosecond rise and fall time, if we accelerate it from 1 nanosecond to 1 picosecond, it will cause stress for switching transistor and loss of efficiency as well. As seen in the Figure 4.4 the gate signal which has 1 nanosecond rise and fall time, causes less than maximum drain current of the switching MOSFET (blue line). On the other hand, the gate signal with a 1 picosecond rise and fall time, causes approximately 350mA current peaks though maximum drain current is less than 1mA. As expected, these current peaks will result in a loss of efficiency.

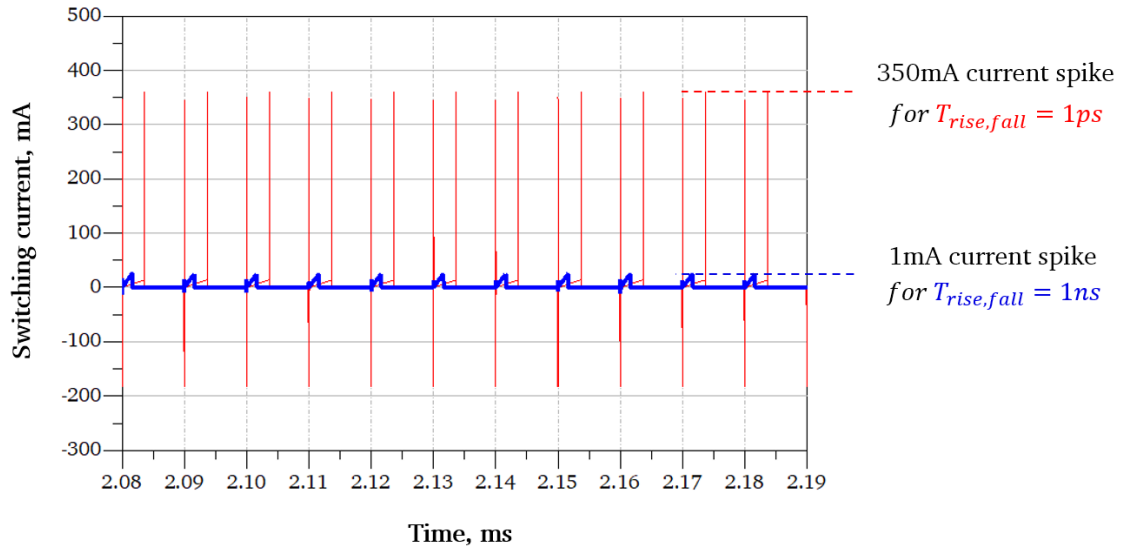


Figure 4.4 Transistor drain currents for different rise and fall times.

4.1.2 Main Converter Efficiency

If we take a look at the efficiency of the converter, we can see a peak efficiency of 81% which occurs at 0.6V input level and 400Ω load. At this point, the converter can deliver 2.79mW power to the output side, while it draws 3.45mW from input. For the whole input span between 0.15V and 1.6V, the converter's average efficiency is 76.7% while the average input power and output power is 3.34mW and 2.57mW respectively. The minimum efficiency, occurring at 0.15V input voltage level, is 66.3%. Efficiency, input and output power levels for the steady state are calculated via equation (4.1) are demonstrated in Figure 4.5.

$$\eta = \frac{P_{out}}{P_{in}} = \frac{\frac{1}{T}\int_0^T v_{out}(t).i_{out}(t)dt}{\frac{1}{T}\int_0^T v_{in}(t).i_{in}(t)dt} \tag{4.1}$$

The green line shows the efficiency levels, the blue line shows the input power drawn from the transducer and the purple line shows the output power transferred to load. Dashed red line drawn vertically shows the boundary input voltage level where the main converter alters the operation mode to DCM from CCM.

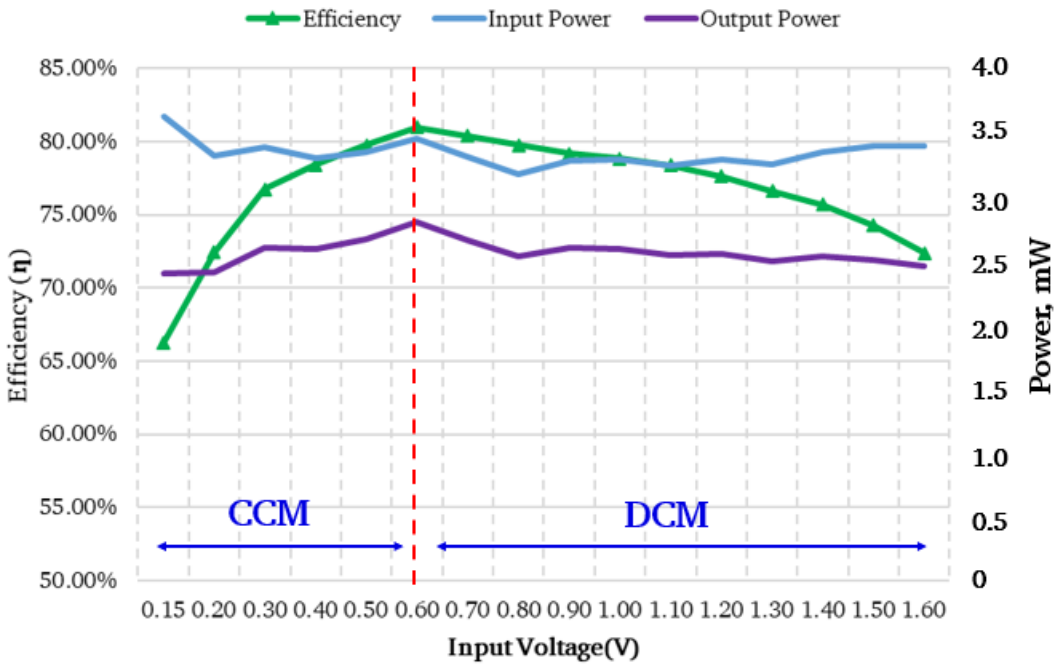


Figure 4.5 Main converter efficiency, input and output power levels

The efficiency levels of the SEPIC Converter according to the load change are shown in Figure 4.6. Below the optimum load value of 400 Ω, the efficiency decreases down to 63% at minimum input voltages and efficiency increases as the voltage rises. On the other hand, above the optimum load value, while the efficiency remains almost the same at low voltages, the efficiency decreases down to 61% as the input voltage increases.

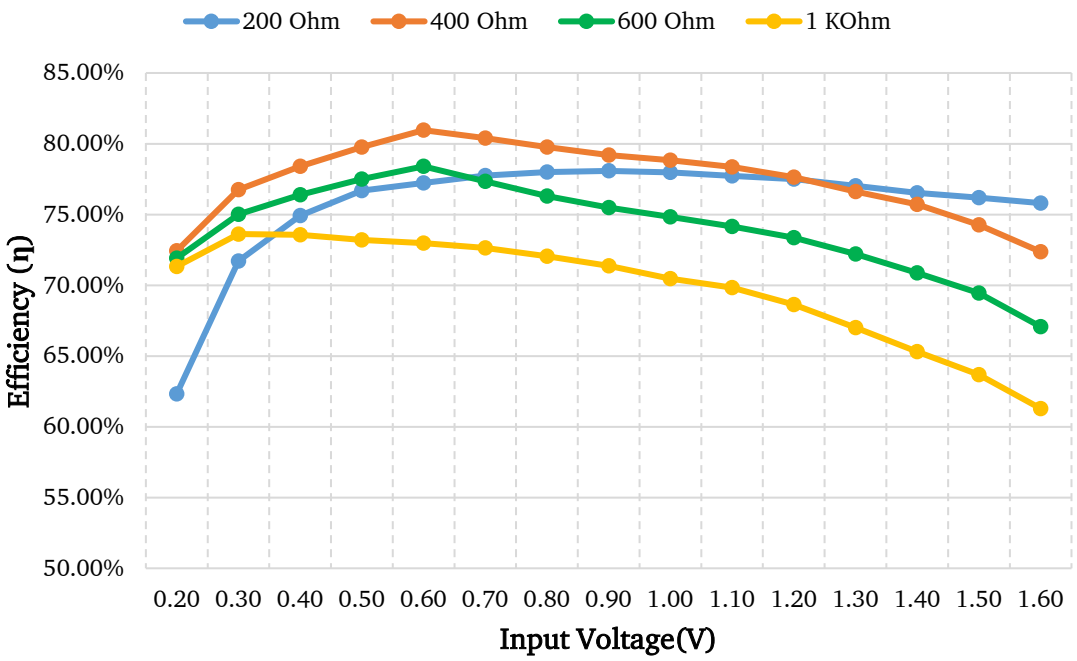


Figure 4.6 Efficiency levels according to load changes

4.1.3 Main Converter Loss Analysis

When we look at the power consumption of the circuit elements, it is seen that the power loss occurs most on the output diode with an average of 16.62% and the highest power loss after the output diode is on the switching transistor with 4.97%. When the duty cycle is the highest and the input voltage is the lowest, the power consumption on the switch is higher due to the relatively more current passing through the switching transistor.

The conduction loss of output diode is expressed as below;

$$P_{Loss(Q2)} = I_D.R_{Q_2DS(on)}.(1-D) \tag{4.2}$$

Where I_D and $R_{Q_2DS(on)}$ are the diode connected NMOS drain-source current and drain-source conduction resistance. Note that reverse losses of the diode connected NMOS are neglected.

While the total loss of the switching transistor Q_1 is the sum of conduction loss and switching loss. The conduction loss and switching loss are calculated with the equation (4.3) and (4.4) respectively.

$$P_{Cond.Loss(Q1)} = I_{Q1}.R_{DS(on)}.D \tag{4.3}$$

$$P_{Sw.Loss(Q1)} = (V_{in,\min} + V_{out}).I_{Q,peak}.\frac{Q_{GD}.f_{sw}}{V_{in,\min}^2} \tag{4.4}$$

Combining equations (4.3) and (4.4), the total loss arising from switching transistor can be expressed as below.

$$P_{Loss(Q1)} = I_{Q1}.R_{DS(on)}.D + (V_{in,\min} + V_{out}).I_{Q,peak}.\frac{Q_{GD}.f_{sw}}{V_{in,\min}^2} \tag{4.5}$$

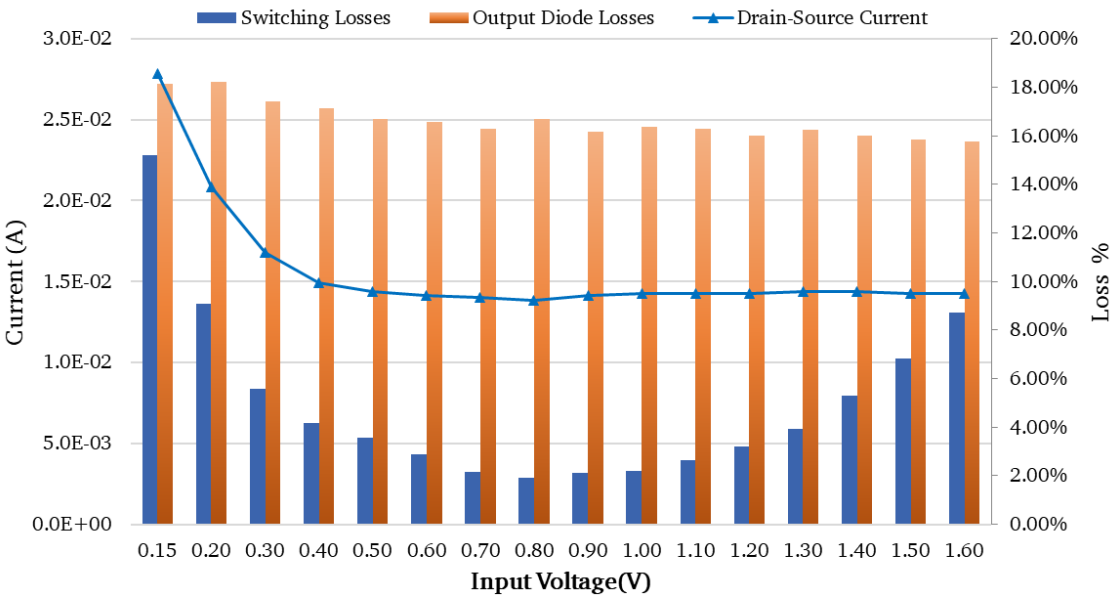


Figure 4.7 Losses of switching transistor and output diode according to input voltages

According to equation (4.5), if we assume the frequency and the output voltage to be constant, losses on the switching transistor is heavily dependent on the drain current and input voltage. As seen in Figure 4.7, for the input voltages between 0.15 and 0.6V, the duty ratio and the “drain-source (IDS)” current are dominant in the losses on the switching transistor. On the other hand, the transistor internal resistance value, which increases with the effect of high drain-source voltage (V_{DS}), is dominant in the 1-1.6V input voltage range. Because of the extremely low input voltages, the switching transistor’s conduction losses are much more dominant than switching losses. Since the transistor switching frequency was chosen relatively low, switching losses were limited at 0.3%.

4.2 Control System Simulation and Analysis

With the need of a robust harvesting system, a fast and effective start-up mechanism, which is not complex and doesn’t easily fail is utilized. Although the main converter is capable of stepping up even a very low input voltage of 0.15V, the ability to operate itself without any external intervention limits the input voltage range considerably. The input voltage level required for the system to take action is 0.5V. As soon as the input voltage reaches 500mV, duty cycle control circuitry begins to adjust duty ratio and keep the output voltage always at 1V level. After start-up, when output voltage reaches 1 V, the system can recover lower input voltages down to 400mV.

To get a better understanding, the signals circulating the whole circuitry should be followed step by step. A single cycle of converting operation of the harvesting system can be summarized briefly for the designated voltage levels of 500mV and 1.2V.

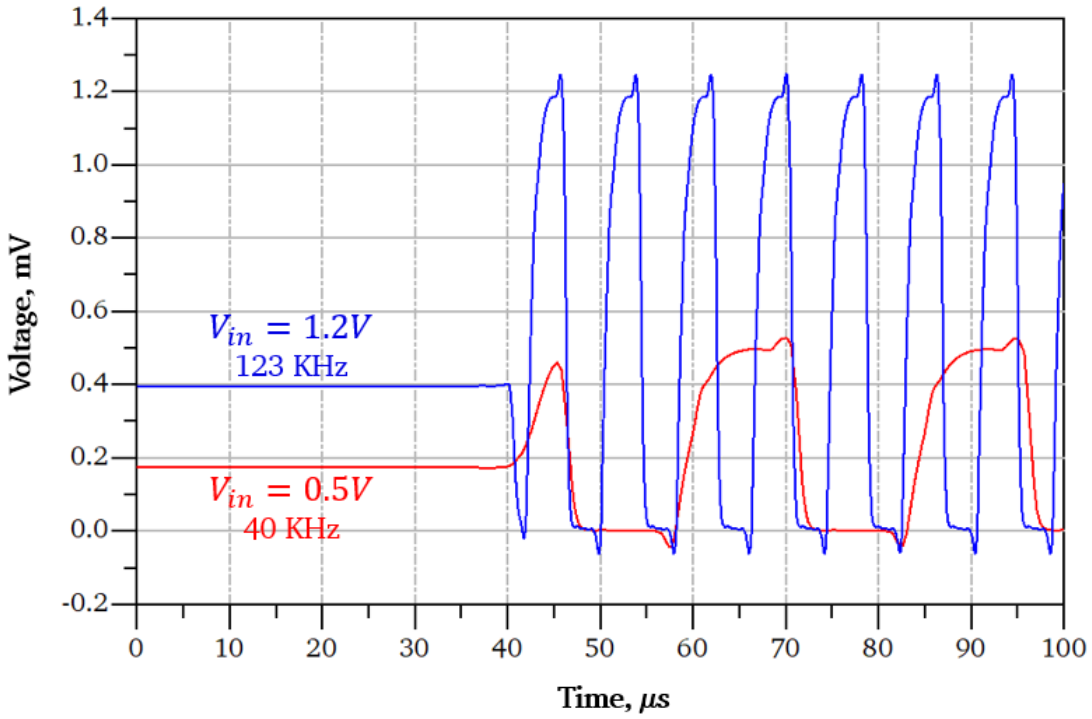


Figure 4.8 Oscillator output signals for 0.5V and 1.2V input voltage levels

The output of the 7-stage ring oscillator for the 0.5V and 1.2V input voltage levels are demonstrated in Figure 4.7. Oscillation starts to take action after 40 microseconds for both input levels and duty cycles are the same as 50%. As stated in equation (3.3), the oscillation frequency only depends on input voltage, since the circuit structure is the same. As a result of the simulations, the oscillation frequency is 40 Khz and 123 Khz for the input voltages 0.5V and 1.2V respectively.

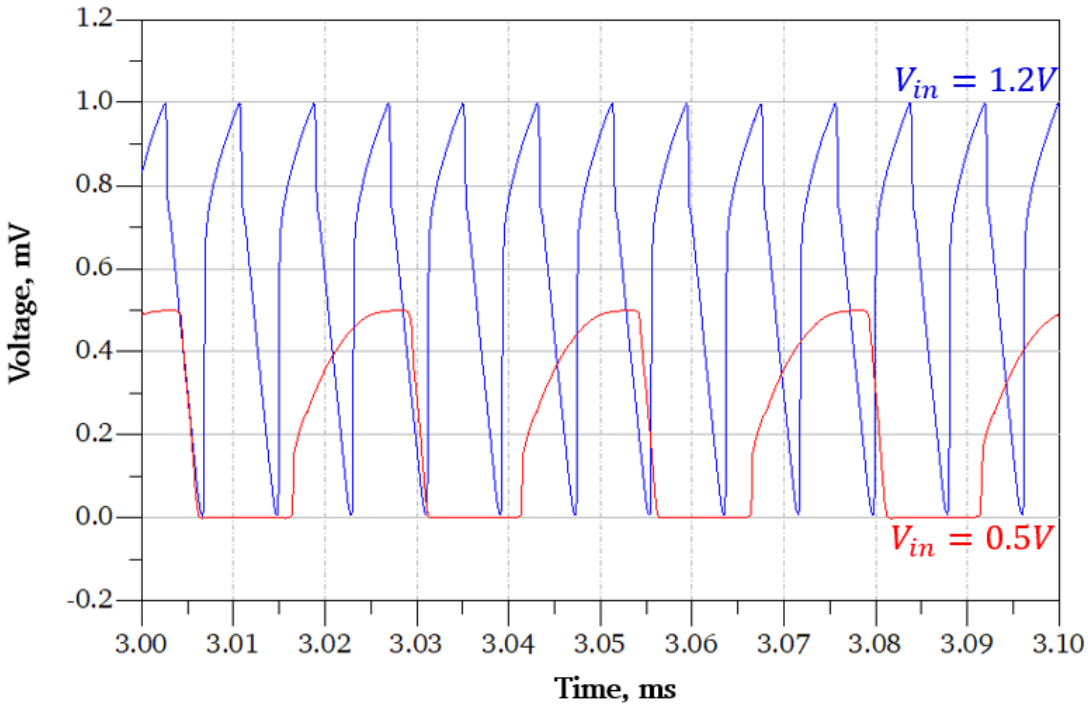


Figure 4.9 Squarewave to trianglewave transformation of 0.5V and 1.2V input voltage levels

After received from the oscillator output, the signal is refined and made more square with an inverter stage and directly fed to the transmission gate stage to transform it into a triangle wave. The transmission gate has a quite large resistance which forces the signal at nearly all relevant frequencies. Therefore, the generated triangle signal, which is demonstrated in Figure 4.8, now allows us to have an altered duty cycle. On the other side, a reference voltage is obtained from a voltage divider which is connected to the converter output.

At this point, the signal obtained from the output of the transmission gate and the reference voltage from the voltage divider are applied to identical inverters individually. These identical inverter outputs are connected together to form a junction point which compares the reference voltage to the triangle wave. The signal generated on the junction point is applied to two inverter stages in series to refine and get a squarer wave. The signal at the end of the control circuitry is now adjusted and ready to be applied to the switching transistor gate. Step signals which are used to bias the transistor are demonstrated in Figure 4.9.

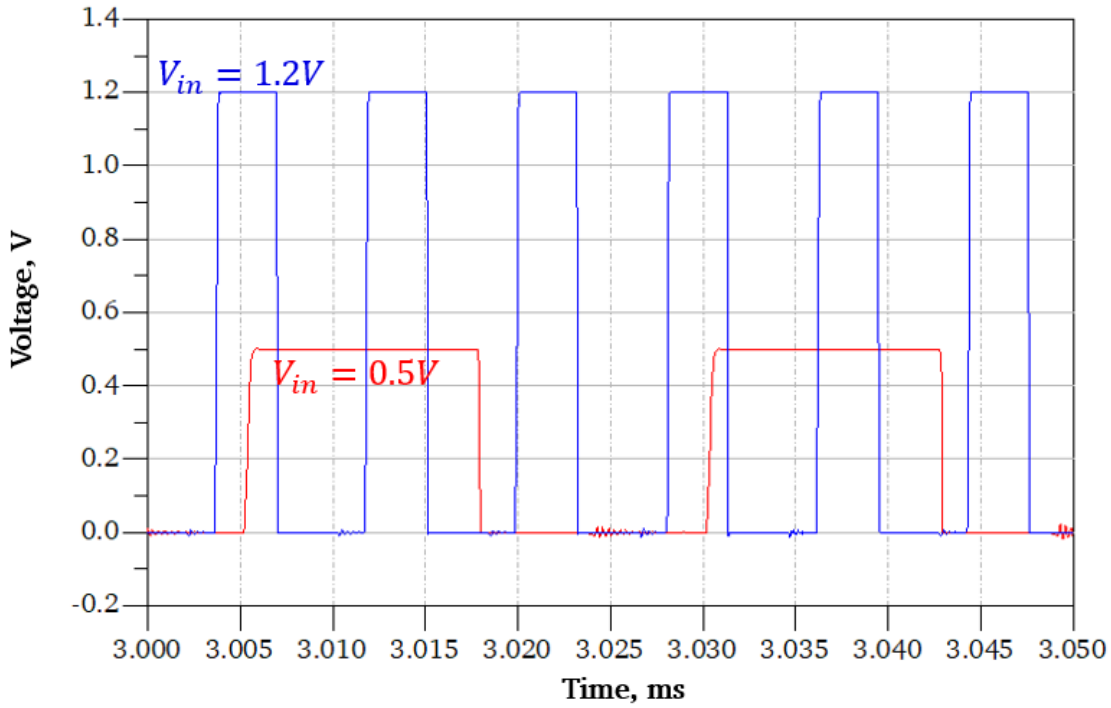


Figure 4.10 Generated clock signals for 0.5V and 1.2V input voltage levels

Finally, the adjusted duty cycle clock signal is ready to be applied to the main converter. Input voltage starting from the 0.5V to 1.6V is can now be converted to output voltage of 1V. The only difference occurring at the output voltage is the voltage ripple which can be seen in Figure 4.10.

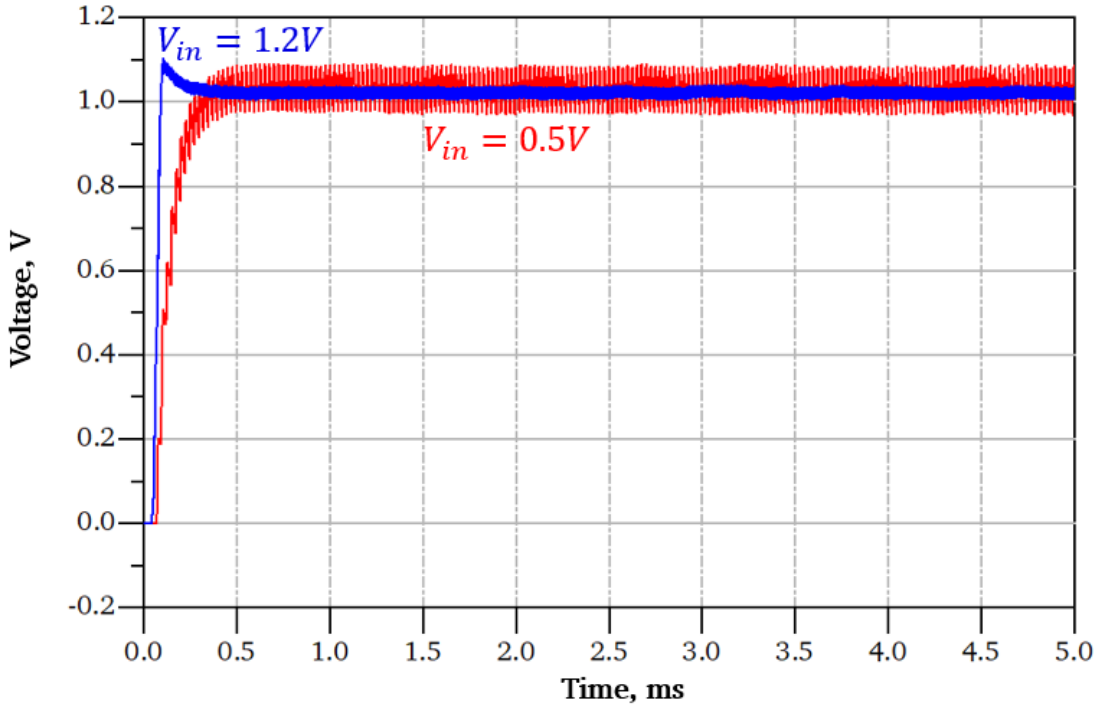


Figure 4.11 DC-DC SEPIC converter output voltages for 0.5V and 1.2V input voltage levels

As seen in the Figure 4.10, the output signal settles down pretty quickly after 0.5 milliseconds after start-up. According to equation (3.2), voltage ripple at the output is dependent on the frequency and input voltage. Therefore, verifying the calculations, the voltage ripples are 0.1V and 0.03V for the input voltages 0.5V and 1.6V respectively.

4.3 Harvesting System End-to-End Simulation

Designed battery-less harvesting system can up and down convert the input voltage between 0.5V and 1.6V supplied by the transducer efficiently. While executing this operation, it does not need any external intervention or pre-charged capacitor. Fundamentally, the basic principle underlying for the system architecture is Harvest and Use. Therefore, there is not any rechargeable battery to store the energy. The whole energy transfer to the load happens instantly and rapidly. For an input signal begins from 0.5V and 1.6V the output voltage is demonstrated in Figure 4.11.

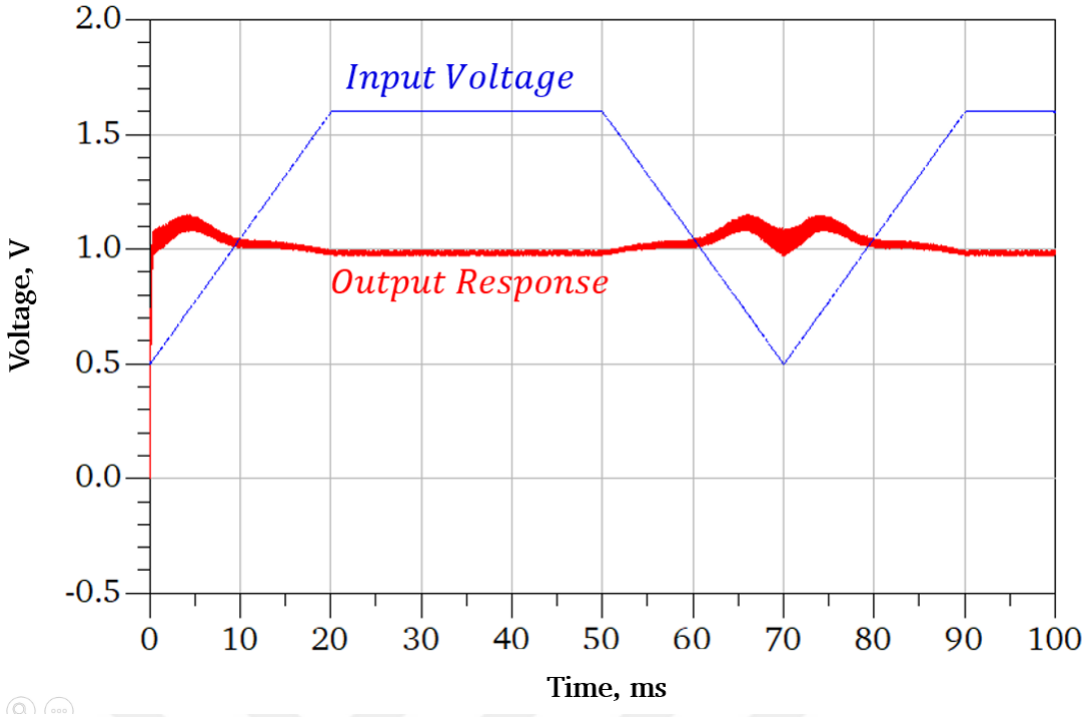


Figure 4.12 Output voltage response for input voltage change

4.3.1 Harvesting System Efficiency

Batteryless harvesting system consisting of a DC-DC SEPIC converter as a main converter has a peak efficiency of 81% corresponding to 0.6V input voltage level. It can be said that the peak efficiency is at a remarkably good level compared to its challenging counterparts.The lowest efficiency is 55.6% which corresponds to 1.6V input voltage level. For all input voltage span, the average efficieny is 69.1%. The power drawn at system input varies between 3.4mW and 4.3mW. On the other hand, the power measured at the output side varies between 3.1mW and 2.4mW. Efficiency, input and output power levels of the overall harvesting system are demonstrated in Figure 4.12.

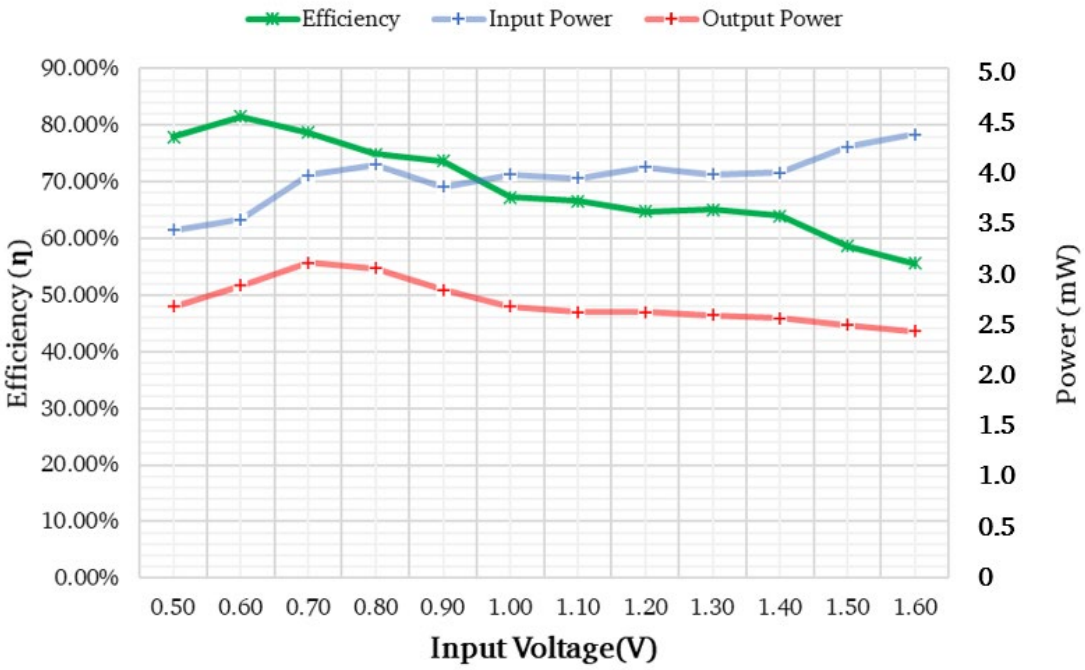


Figure 4.13 Efficiency, input and output power of overall system.

While the overall efficiency level is as stated above, the oscillator and duty cycle control circuitry power consumption do not have a significant effect on overall efficiency. Considering the 0.5V input voltage level the average consumption of the oscillator is only 9.6nW, where the consumption for the 1.2V input voltage level increases up to 250nW. On the other hand, for 0.5 input voltage level the average consumption of the duty cycle control circuitry is 290nW, while the consumption for the 1.2V input voltage level is 19μW. The power consumptions of both oscillator and duty cycle control circuitry increase as the input voltage increases. In Figure 4.13 and Figure 4.14, oscillator power consumptions and duty cycle control circuitry power consumptions are demonstrated respectively.

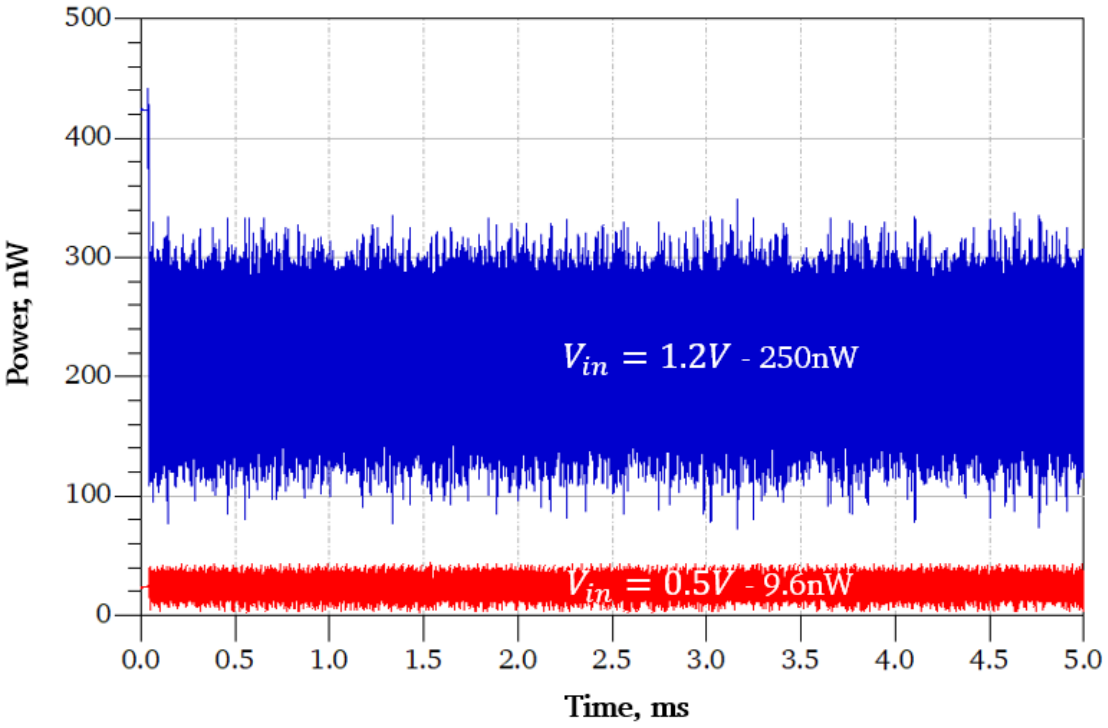


Figure 4.14 Power consumption of oscillator for 0.5V and 1.2V input voltage levels.

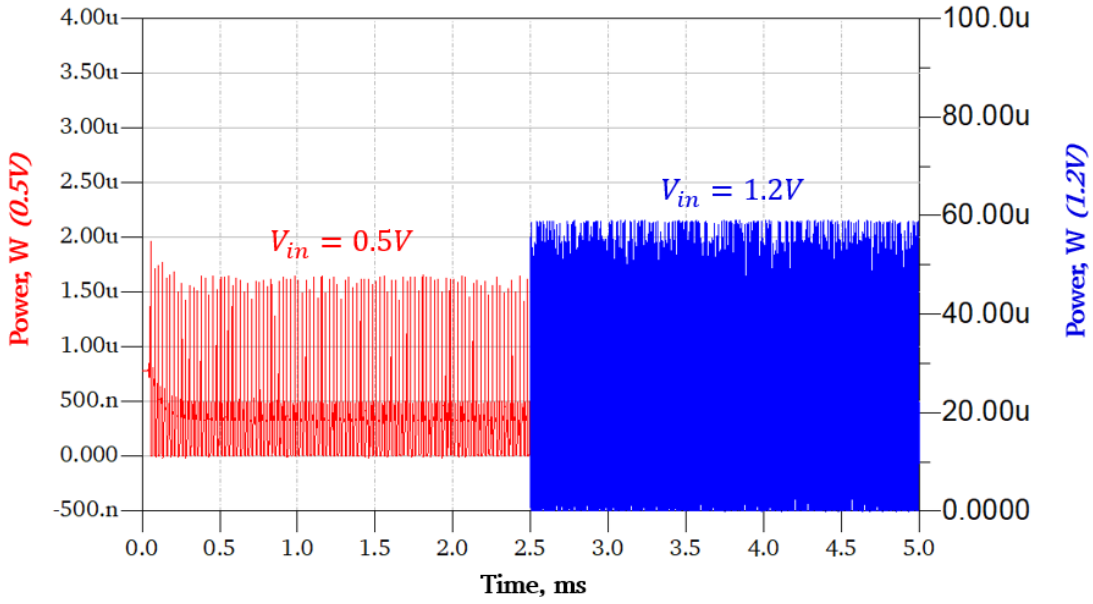


Figure 4.15 Power consumption of duty cycle control circuitry for 0.5V and 1.2V input voltage levels

5
RESULTS AND DISCUSSION

In EH's challenging world, it is important to constantly improve and create flexible structures. There is a vast variety of power requirements of immense diversity. In this thesis, it is aimed to make a harvesting system with the practical SEPIC converter which can start-up itself, cover the maximum input voltage, capable of delivering a continuous and reliable voltage and as efficient as possible. On the other hand, it is aimed to investigate the use of DC-DC SEPIC converter in energy harvesting applications powered by thermoelectric and photovoltaic energy. Utilizing the SEPIC converters and duty cycle control circuitry together, this study is unique for the usage of SEPIC converter for energy harvesting purposes.

For comparing considerations, within our knowledge, the most similar three studies from the literature are demonstrated in Table 5.1. In [9], a single inductor dual-input-dual-output structure is demonstrated for PV and PE harvesting. Although it achieves a good efficiency level of 88%, a battery is used in the design to ensure operating continuity. Among the competitors, the only example utilizes SEPIC converter for very low voltage purposes that aims MPPT for TEG energy harvesting [15], presents a relatively restricted input voltage span and low efficiency. Another study, which can be presented as a different topology, designed in 130nm process, utilizes charge pumps and charge transfer switches for stepping up voltage [33]. It also consists of start-up capacitors to store energy for starting up. Although it presents multiple outputs, the presented system has very low output power compared to this work. In [34], the input voltage range is not stated but it is stated that for the 200mV input voltage the corresponding output voltage is 1.1V. Although it has a remarkable start up voltage, the peak efficiency for this input voltage is declared to be 63%. When we look at the start-up circuits, the oscillator topology used in this work is similar to [33] which is a ring oscillator. On the other hand, in [34] an inductor based LC oscillator is used instead.

Table 5.1 Comparison of the most similar energy harvesting applications

	[9]	[15]	[33]	[34]	This Work
Input Voltage	2-3.3V	0.5-1V	-	0.2V	0.5-1.6 V
Design Process and Topology	180nm Integrated	Discrete SEPIC	Partially Integrated CP+Boost 130nm	180nm Integrated LC Osc. +Boost	Partially Integrated SEPIC 130nm
Converting Direction	Bi-directional	Bi-directional	Bi-directional	Step-Up	Bi-directional
Switching Frequency	1 MHz	94 KHz	-	-	40-123 KHz
Output Voltage	1.8V, 3.3V	0.8V	0.5V, 1, 1.8V	1.1V	1 V
Load	-	5-20Ω	-	-	400Ω
Output Power	180mW	-	1-100μW	1μW-2mW	2.4-3.1mW
Peak Efficiency	%88	%69	%71	%63	%81
Start-Up	Yes	No	Yes	Yes	Yes

Though minimum input voltage, which can be boosted, is not very competitive, this study is superior in terms of efficiency and input voltage range. To further improve this energy harvesting system by adding another set of sub-circuits, the start-up voltage can be reduced, efficiency can be improved and clear up the impedance matching issues. By adding a supercapacitor and rechargeable battery, a Harvest-Store-Use topology can be designed. Already, the presented harvesting system can provide reliable power for wireless sensors etc. As a result, this study has reached its goal as it shows that the SEPIC converter can be used efficiently in very low voltage energy harvesting applications. For future work, a charge pump stage will be added to lower the minimum input voltage down to 100-200mV levels.

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A
TRANSISTOR SIZING

The metal-oxide-semiconductor (MOS) is composed of silicon dioxide (SiO_2) on top of a silicon substrate which consist of n-type and p-type materials. Between the source and drain is formed a channel where the current flow through. The width of this current flowing channel named as the ***Width*** of the transistor and the length is named as the ***Length*** of transistor as well.

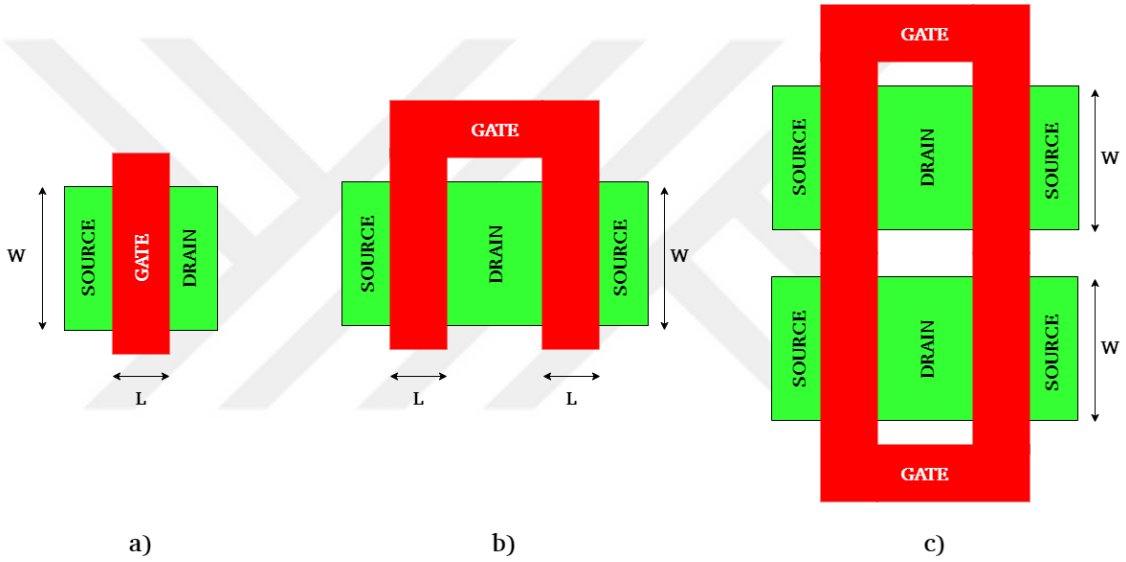


Figure A.1 Transistor finger and multiplier function

In layout drawings, transistors are divided and multiplied so that large transistors do not take up space and are produced in a squarer structure. In addition, this process has advantages in that it reduces the gate resistance and current density. Assume we have a single transistor sized as W/L in Figure A.1 (a) having finger=1 and multiplier=1;

- The transistor width can be sized as 2W by applying Finger=2 and Multiplier=1 demonstrated in Figure A.1 (b).
- The transistor can be doubled and sized as 4W in total by applying Finger=2 and Multiplier=2 demonstrated in Figure A.1 (c).

B
7-STAGE RING OSCILLATOR DESIGN CALCULATIONS

Table B.1 Stage ring oscillator design parameters

Parameter	Symbol	Value
Vacuum Permittivity	ε_o	$8.854\times10^{-12}\,F/m$
Relative Permittivity (Silicon dioxide)	ε_r	-
Surface Mobility (NMOS)	μ_n	$0.04155 m^2/V.s$
Surface Mobility (PMOS)	μ_p	$0.01205 m^2/V.s$
Oxide Thickness (PMOS)	t_{ox}	$2.73\times10^{-9}\,m$
Threshold Voltage (NMOS)	V_{THn}	$2.16\times10^{-1}V$
Threshold Voltage (PMOS)	V_{THp}	$2.5\times10^{-1}V$
Threshold Voltage (Equivalent)	V_{TH}	$2.34\times10^{-1}V$
PMOS/NMOS Scaling Ratio	k	-
Supply Voltage	V_{DD}	$8\times10^{-1}V$
Length	m	$47\times10^{-6}\,m$

Considering above parameters, which have been derived from UMC 130nm technology datasheets of “1P8M High Speed Enhancement 1.2V MOSFET”, the ring oscillator frequency is calculated below. To get a better understanding and simplicity, the deviations of some parameters are neglected.

C_{ox}, oxide capacitance;

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.9 \times 8.854 \times 10^{-12} F/m}{2.73 \times 10^{-9} m} = 12.65 \times 10^{-3} F/m^2$$

K_{pn}, transconductance coefficient of NMOS;

$$K_{pn} = \mu_n C_{ox} = 0.04155 m^2/V.s \times 12.65 \times 10^{-3} F/m^2 = 525.6 \times 10^{-6} F/V.s$$
$$K_{pn} = 525.6 \times 10^{-6} A/V^2 = 525.6 \mu A/V^2$$

K_{pp}, transconductance coefficient of PMOS;

$$K_{pp} = \mu_p C_{ox} = 0.01205 m^2/V.s \times 12.65 \times 10^{-3} F/m^2 = 152.43 \times 10^{-6} F/V.s$$
$$K_{pp} = 152.43 \times 10^{-6} A/V^2 = 152.43 \mu A/V^2$$

τ_p, inverter delay from equation (3.4);

$$\tau_p = \frac{2 \times 12.65 \times 10^{-3} \times (47 \times 10^{-6})^2 (1+1)(0.8 - 2(0.234)}{(0.8 - 0.234)^2} \times \left(\frac{1}{1 \times 152.43 \times 10^{-6}} + \frac{1}{525.6 \times 10^{-6}} \right) = 9.8 \times 10^{-7} s$$

f_0, oscillating frequency of the ring oscillator from equation (3.3);

$$f_0 = \frac{1}{2 \times 7 \times 9.8 \times 10^{-7}} \cong 73 KHz$$

PUBLICATIONS FROM THE THESIS

Conference Papers

1. İ. Güzeltepe, R. A. Vural and O. Z. Batur, "130nm DC-DC SEPIC Design and analysis for Energy Harvesting Applications," 2020 12th International Conference on Electrical and Electronics Engineering (ELECO), Bursa, Turkey, 2020, pp. 103-107, doi: 10.1109/ELECO51834.2020.00041.