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Modified Gorski-Popiel Technique and Synthetic Floating Transformer Circuit Using Minimum Components*

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The aim of this paper is proposing an alternative method to Gorski-Popiel Technique in realization of synthetic transformers. A new synthetic floating transformer (FT) circuit is also given. The proposed synthetic transformer circuit uses two current backward transconductance amplifiers (CBTAs), three resistors, and two grounded capacitors. The primary self-inductance, the secondary self-inductance, and the mutual inductance can be independently controlled and can be tuned electronically by changing the biasing current of the employed CBTAs. It has a good sensitivity performance with respect to tracking errors. A band-pass filter is also realized to test the performance of the proposed synthetic transformer circuit. The validity of the proposed synthetic transformer circuit is demonstrated by PSPICE simulations and experimental results.

Keywords: Modified Gorski-Popiel technique; synthetic transformer; mutually coupled circuits; current backward transconductance amplifier; active circuits; band-pass filter.

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1. Introduction

Synthetic transformer circuits are widely used in communication, instrumentation, and control. They can also be used for analog filters, particularly for replacing the magnetic transformer in stagger-tuned filters. A mutually coupled circuit comprises a primary self-inductance L_p, a secondary self-inductance L_s, and a mutual inductance M. Due to process tolerances in IC fabrication, the inductance values may differ from run to run. Moreover, since they require substantial chip area, and huge process cost, they are not feasible for IC implementations. Therefore, the advent of integrated circuits has encouraged the design of synthetic transformer, which can be used instead of the physical transformers in integrated circuits.

A literature survey reveals that several studies have been proposed for simulating a mutually coupled circuit using conventional operational amplifiers,[1–3] bipolar junction transistors,[4,5] second-generation current-conveyors (CCIIs),[5–8] and the operational transconductance amplifiers (OTAs).[5,9] However, the implementation of synthetic transformers using current-conveyor and current-conveyor-based active component has been of much attention for their potential advantages such as higher signal bandwidths, greater linearity, wider dynamic range, simple circuitry, and low power consumption.[10]

Further, many of the proposed synthetic transformers circuits require so many active and passive components and require several passive component matching constraints.[3,6] Abulma'atti *et al.* proposed a transformer circuit in 2005.[7] It requires six CCIIs, six resistors, and two capacitors. The circuit proposed by Yuce and Minaei employs four second-generation current controlled conveyors (CCCIIs), five resistors, and two capacitors.[8] Another proposed circuit[11] uses two dual-output CCCIIs (DO-CCCIIs) and three CCCIIs in its main structure together with one plus-type CCII (CCII+) and one minus-type CCII (CCII−) for realization of an inductance. Two different mutually coupled circuits are also presented by Gunes *et al.*[12] The first circuit employs four OTAs (two of them dual-output OTAs (DO-OTAs)), two resistors, and two capacitors.[12] Alternatively, the second one uses two differential voltage current-conveyors (DVCCs) and two CCII+s together with six resistors and two capacitors. It is important to note that besides the disadvantages of excessive number of active and passive elements, all of the above-mentioned structures realize only grounded synthetic transformer. In some application such as filters it is required to use floating-type transformers. So, the circuit proposed by Koksal *et al.* uses three current backward transconductance amplifiers (CBTAs) and grounded capacitors to realize a floating-type transformer.[13] There have been also several studies on the floating simulated inductance circuits in the literature so far.[14–26] It should be mentioned that a synthetic floating transformer (FT) can be alternatively realized by using three floating simulated inductors that are connected as T-type model. However, such synthetic transformers employ a large number of active and passive components.

Table 1. Comparison of the synthetic transformers.

Ref.	No. of active elements	Synthetic transformer	No. of C	No. of R
5	Circuit 1: 8 CCIIs	Grounded	4	6
	Circuit 2: 4 CCIIs and 2 OTAs	Grounded	4	4
	Circuit 3: 6 OTAs	Grounded	2	2
	Circuit 4: 8 OTAs	Grounded	2	—
7	6 CCII+s	Grounded	2	6
8	4 CCCIIs	Grounded	2	5
11	2 DO-CCCIIs, 3 CCCIIs, 1 CCII+ and 1 CCII−	Grounded	2	—
12	Circuit 1: 2 OTAs and 2 DO-OTAs	Grounded	2	6
	Circuit 2: 2 DVCCs and 2 CCII+s	Grounded	2	6
13	3 CBTAs	Floating	3	—
Proposed	2 CBTAs	Floating	2	3

In this work, a new synthetic transformer circuit is presented. The proposed synthetic transformer circuit uses two CBTAs, three resistors, and two grounded capacitors.

The primary self-inductance, the secondary self-inductance, and the mutual inductance can be independently controlled and can be tuned electronically. More importantly, the proposed circuit realizes floating-type transformer which makes it superior to most of the previously published ones. The proposed synthetic transformer is compared with the synthetic transformer reported in the literature and the result is shown in Table 1.

The validity of the proposed circuits is demonstrated by PSPICE simulations and experimental results.

2. Current Backward Transconductance Amplifier

A recent publication introduces the concept and implementation of a circuit building block termed CBTA.[27] CBTA is proven to be useful in many voltage-mode and current-mode analog signal processing applications, such as current-mode filters, voltage-mode filters, and immittance function simulators.[13,23,24,27–31] The circuit symbol of CBTA is shown in Fig. 1(a)[27] where p and n are input terminals and w and z are output terminals. This active element is equivalent to the circuit in Fig. 1(b), which involves dependent current and voltage sources. The CBTA terminal equations can be defined as Eq. (1):

$$I_z = g_m(s)(V_p - V_n)\,, \quad V_w = \mu_w(s)V_z\,, \quad I_p = \alpha_p(s)I_w\,, \quad I_n = -\alpha_n(s)I_w\,, \qquad (1)$$

where $\alpha_p(s)$, $\alpha_n(s)$, and $\mu_w(s)$ are the current and voltage gains, respectively. $g_m(s)$ is the transconductance gain. They can be expressed as: $\alpha_p(s) = \omega_{\alpha p}(1-\varepsilon_{\alpha p})/(s+\omega_{\alpha p})$, $\alpha_n(s) = \omega_{\alpha n}(1-\varepsilon_{\alpha n})/(s+\omega_{\alpha n})$, $g_m(s) = g_o\omega_{gm}(1-\varepsilon_{gm})/(s+\omega_{gm})$, and $\mu_w(s) = \omega_\mu(1-\varepsilon_\mu)/(s+\omega_\mu)$ with $|\varepsilon_{\alpha p}| \ll 1$, $|\varepsilon_{\alpha n}| \ll 1$, $|\varepsilon_{gm}| \ll 1$, and $|\varepsilon_\mu| \ll 1$.

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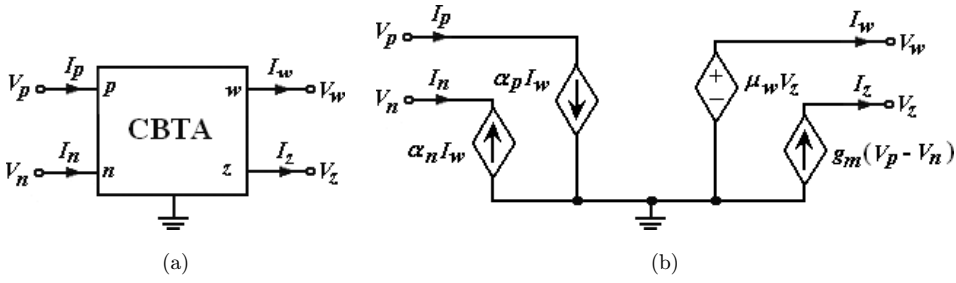


Fig. 1. (a) Block diagram of CBTA and (b) equivalent circuit of CBTA.

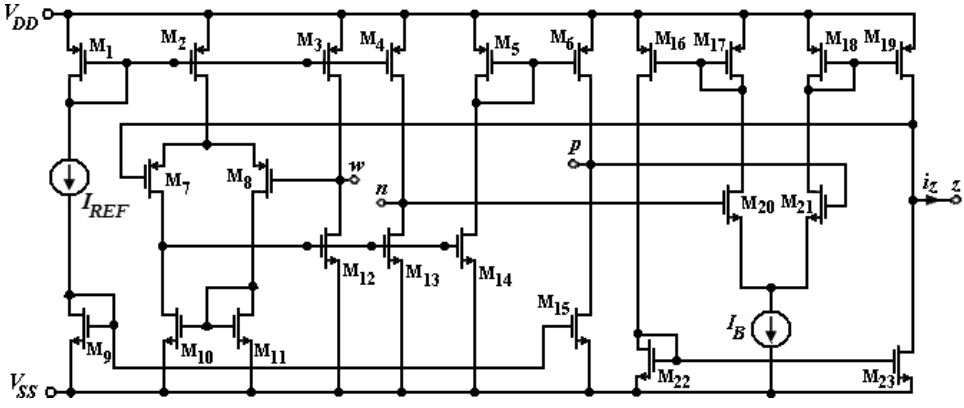


Fig. 2. CMOS implementation of CBTA.

Here, g_o is the DC transconductance gain, $\varepsilon_{\alpha p}$ and $\varepsilon_{\alpha n}$ are the current tracking errors, ε_μ is the voltage tracking error, and ε_{gm} denotes transconductance error. In addition, $\omega_{\alpha p}$, $\omega_{\alpha n}$, ω_{gm}, and ω_μ denote corner frequencies of the relevant parameter. Note that, in the ideal case, the voltage and current gains are equal to unity, i.e., $\mu_w(s) = 1$ and $\alpha_p(s) = \alpha_n(s) = 1$.

The CMOS implementation of CBTA which consists of transconductance[32] and current-conveyor sections[12] is given in Fig. 2. It is obtained by connecting appropriate outputs of these sections and adjusting the dimensions of CMOS transistors. The dimensions of the MOS transistors used in CBTA implementation are given in Table 2.

In Fig. 2, the transconductance section is realized by using the transistors M_{16}–M_{23} that are formed by MOS coupled pair and current mirrors. v_{in} is the differential input voltage ($v_{in} = v_p - v_n$), i_z is the output current of the transconductance section, and I_B is the bias current. It is assumed that all MOS devices operate in the saturation region. Assuming that M_{20} and M_{21} are perfectly matched and the current

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Table 2. Dimensions of the CMOS transistors.

PMOS transistors	W (μm)/L (μm)
M_1–M_4	7.2/0.36
M_5–M_8	3.6/0.36
M_{16}–M_{19}	5.76/1.44
NMOS transistors	W (μm)/L (μm)
M_9 and M_{13}–M_{15}	3.6/0.36
M_{10} and M_{11}	1.8/0.36
M_{20} and M_{21}	18/1.44
M_{22} and M_{23}	2.88/1.44

mirrors have unity current gain, i_z can be given by

$$i_z = g_m v_{\text{in}} = (\sqrt{2I_B K}) v_{\text{in}}\,, \tag{2}$$

where $K = \mu C_{\text{ox}} W/2L$, μ is the mobility of the carrier, C_{ox} is the gate-oxide capacitance per unit area, W is the effective channel width, and L is the effective channel length.

3. Modified Gorski-Popiel Technique

The Gorski-Popiel technique is a special case of generalization of the inductor simulation method by the use of general impedance converter (GIC).[33,34]

Figure 3(a) shows the simplified representation of GIC. The relationship between the currents and the voltages of GIC input and output ports is as follows:

$$V_2(s) = V_1(s)\,, \quad I_2(s) = sTI_1(s)\,, \tag{3}$$

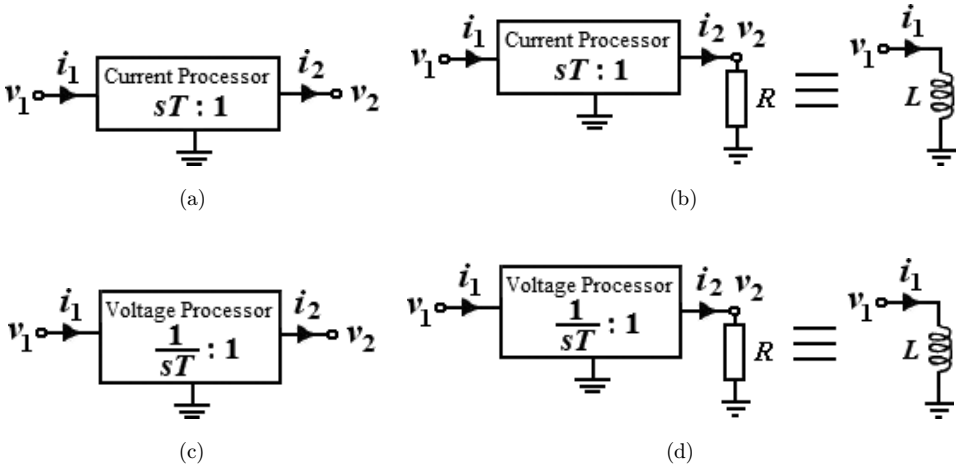


Fig. 3. (a) The block diagram of GIC, (b) converting a resistor R to an inductor TR, (c) the block diagram of modified GIC and (d) converting a resistor R to an inductor TR.

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where T is a time constant that is a characteristic of GIC. If the resistor R is connected to the output port of GIC as shown in Fig. 3(b), we can write

$$V_2(s) = V_1(s) = RI_2(s) = sTRI_1(s)\,, \tag{4a}$$

and the input impedance of the circuit can be found as follows:

$$Z_{\text{in}}(s) = V_1(s)/I_1(s) = sTR\,. \tag{4b}$$

Thus the resulting circuit operates as a grounded inductor simulator with $L = TR$. The classical approach shown in Fig. 3(a) is based on transferring of the input voltage to the output and taking a differential of the input current and transferring it to the output as defined above. The proposed method is based on transferring the input current to the output and taking an integral of the nonideal coupling coefficient of the input voltage and transferring it to the output. Figure 3(c) shows the modified representation of GIC which is characterized by the following equations:

$$V_2(s) = (1/sT)V_1(s)\,, \quad I_2(s) = I_1(s)\,. \tag{5}$$

If a resistor R is connected to the output port of the modified GIC as shown in Fig. 3(d), the input impedance of the circuit is

$$Z_{\text{in}}(s) = V_1(s)/I_1(s) = sTR\,, \tag{6}$$

which represents a grounded inductance with $L = TR$.

To demonstrate that this process is not limited to single resistors or even to n-port networks, consider the resistive n-port in Fig. 4(a). Equation (7) is the relationship between the voltage and current of the n-port resistor circuit and describes the z-parameters of the n-port resistor circuit shown in Fig. 4(a):

$$\begin{bmatrix} V_{1R} \\ V_{2R} \\ \vdots \\ V_{nR} \end{bmatrix} = \begin{bmatrix} R_1 + R_{n+1} & R_{n+1} & \cdots & R_{n+1} \\ R_{n+1} & R_2 + R_{n+1} & \cdots & R_{n+1} \\ \vdots & \cdots & \ddots & \vdots \\ R_{n+1} & R_{n+1} & \cdots & R_n + R_{n+1} \end{bmatrix} \begin{bmatrix} I_{1R} \\ I_{2R} \\ \vdots \\ I_{nR} \end{bmatrix} \tag{7}$$

or

$$\mathbf{V_R} = \mathbf{RI_R}\,, \tag{8}$$

where $\mathbf{V_R}$ and $\mathbf{I_R}$ are the voltage and current column vectors and $\mathbf{R}$ is the resistor matrix indicated in Eq. (7). The modified GIC embedding process with $I_{iR} = I_i$ and $V_{iR} = (1/sT_i)V_i$ $(i = 1, 2, \ldots, n)$ yields

$$\begin{bmatrix} V_1(s) \\ V_2(s) \\ \vdots \\ V_n(s) \end{bmatrix} = s\mathbf{T} \begin{bmatrix} R_1 + R_{n+1} & R_{n+1} & \cdots & R_{n+1} \\ R_{n+1} & R_2 + R_{n+1} & \cdots & R_{n+1} \\ \vdots & \cdots & \ddots & \vdots \\ R_{n+1} & R_{n+1} & \cdots & R_n + R_{n+1} \end{bmatrix} \begin{bmatrix} I_1(s) \\ I_2(s) \\ \vdots \\ I_n(s) \end{bmatrix}, \tag{9}$$

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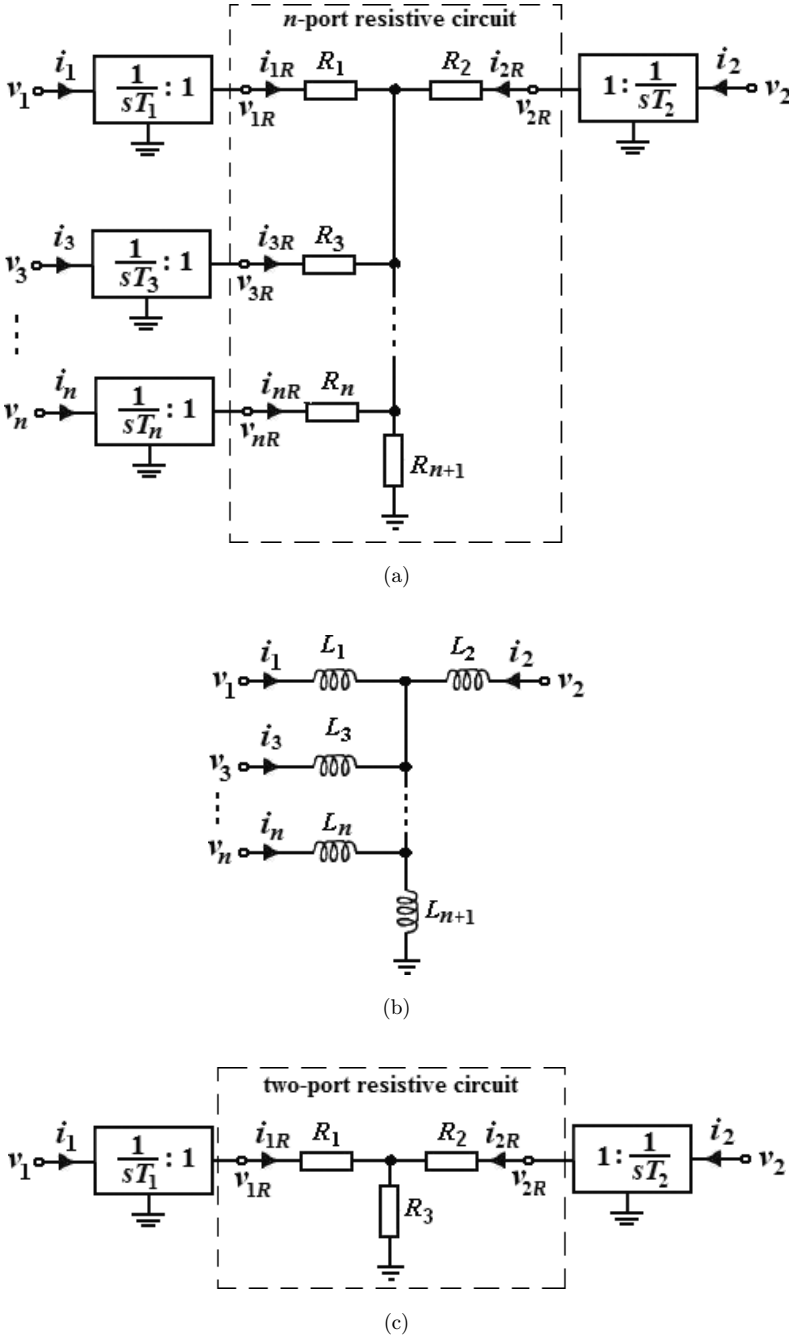
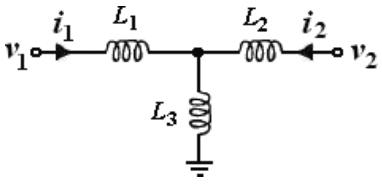


Fig. 4. (a) The n-port resistor network embedded in modified GICs, (b) its equivalent circuit, (c) two-port resistor network embedded in modified GICs and (d) its equivalent circuit.



(d)

Fig. 4. (*Continued*)

where $\mathbf{T}$ is an $n \times n$ matrix given as follows:

$$\mathbf{T} = \begin{bmatrix} T_1 & 0 & \cdots & 0 \\ 0 & T_2 & \cdots & 0 \\ \vdots & \cdots & \ddots & \vdots \\ 0 & 0 & \cdots & T_n \end{bmatrix}. \tag{10}$$

If $T_1 = T_2 = \cdots = T_n$, Eq. (9) describes an inductor circuit shown in Fig. 4(b), where $\mathbf{L} = \mathbf{TR}$ is the inductor matrix:

$$\mathbf{L} = \begin{bmatrix} L_1 + L_{n+1} & L_{n+1} & \cdots & L_{n+1} \\ L_{n+1} & L_2 + L_{n+1} & \cdots & L_{n+1} \\ L_{n+1} & \cdots & \ddots & L_{n+1} \\ L_{n+1} & L_{n+1} & \cdots & L_n + L_{n+1} \end{bmatrix}. \tag{11}$$

Therefore, the relationship between the voltage and current of the two-port resistor circuits shown in Fig. 4(c) are found as follows:

$$\begin{bmatrix} V_{1R} \\ V_{2R} \end{bmatrix} = \begin{bmatrix} R_1 + R_3 & R_3 \\ R_3 & R_2 + R_3 \end{bmatrix} \begin{bmatrix} I_{1R} \\ I_{2R} \end{bmatrix}. \tag{12}$$

After combining this network with the modified GICs as shown in Fig. 4(c) and using Eq. (5), we obtain

$$V_1(s) = sT_1(R_1 + R_3)I_1(s) + sT_1R_3I_2(s)\,, \tag{13a}$$

$$V_2(s) = sT_2R_3I_1(s) + sT_2(R_2 + R_3)I_2(s)\,. \tag{13b}$$

If $T_1 = T_2$, Eqs. (13a) and (13b) describe inductor circuit in Fig. 4(d).

4. Proposed Circuit Configuration and its Analysis

The symbol of the transformer and its equivalent circuit (T-model) are given in Figs. 5(a) and 5(b), respectively. The transformer can be modeled by a two-port network with the following matrix equation:

$$\begin{bmatrix} V_1(s) \\ V_2(s) \end{bmatrix} = \begin{bmatrix} sL_p & sM_{12} \\ sM_{21} & sL_s \end{bmatrix} \begin{bmatrix} I_1(s) \\ I_2(s) \end{bmatrix} \tag{14a}$$

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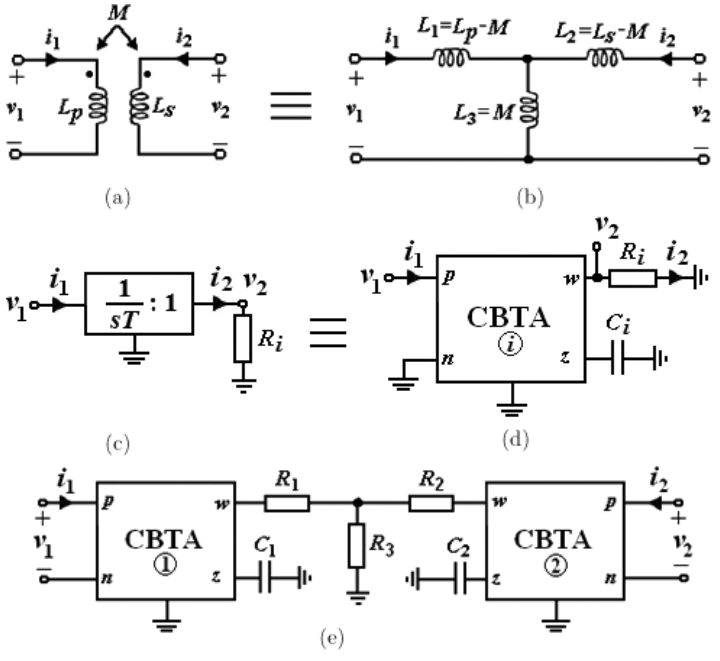


Fig. 5. (a) Symbol of the transformer, (b) equivalent circuit of the transformer, (c) modified GIC-based inductor, (d) CBTA-based circuit of (c) and (e) proposed synthetic floating transformer circuit.

or

$$\begin{bmatrix} V_1(s) \\ V_2(s) \end{bmatrix} = s \begin{bmatrix} L_1 + M_{11} & M_{12} \\ M_{21} & L_s + M_{22} \end{bmatrix} \begin{bmatrix} I_1(s) \\ I_2(s) \end{bmatrix}, \tag{14b}$$

where L_p and L_s are the primary and secondary self-inductances of the transformer, respectively. Here, $L_p = L_1 + M_{11}$ and $L_s = L_2 + M_{22}$, M_{12} and M_{21} are the mutual inductances of the transformer. The condition $M_{11} = M_{22} = M_{12} = M_{21} = M$ is necessary in order to ensure symmetrical coupling. Therefore, inductance values of the equivalent circuit of the transformer which is shown in Fig. 5(b) are found as $L_1 = L_p - M$, $L_2 = L_s - M$.

The proposed modified GIC-based inductor and its simulator circuit using CBTA are shown in Figs. 5(c) and 5(d), respectively. Routine analysis of Fig. 5(d) gives the following equations:

$$I_2(s) = I_1(s)\,, \tag{15a}$$

$$V_2(s) = g_{mi} V_1(s)(1/sC_i) = (1/sT_i)V_1(s)\,. \tag{15b}$$

where $T_i = C_i/g_{mi}$. Using the circuit of Fig. 5(d) in the two-port resistor network of Fig. 4(a) gives the proposed simulated transformer circuit shown in Fig. 5(e).

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Routine analysis of the circuit in Fig. 5(e) yields

$$V_1(s) = s\frac{C_1}{g_{m1}}(R_1 + R_3)I_1(s) + s\frac{C_1R_3}{g_{m1}}I_2(s)\,, \tag{16a}$$

$$V_2(s) = s\frac{C_2R_3}{g_{m2}}I_1(s) + s\frac{C_2}{g_{m2}}(R_2 + R_3)I_2(s)\,. \tag{16b}$$

Comparing (16a) and (16b) with (14) gives the equivalent inductances of the network as

$$L_1 = \frac{C_1R_1}{g_{m1}}, \quad M_{11} = M_{12} = \frac{C_1R_3}{g_{m1}}\,, \tag{17a}$$

$$L_2 = \frac{C_2R_2}{g_{m2}}, \quad M_{22} = M_{21} = \frac{C_2R_3}{g_{m2}}\,. \tag{17b}$$

and

$$L_p = \frac{(R_1 + R_3)C_1}{g_{m1}}, \quad L_s = \frac{(R_2 + R_3)C_2}{g_{m2}}\,. \tag{17c}$$

The inductances L_1, L_2, and M can be independently controlled by changing the resistors R_1, R_2, and R_3, or g_{mi} $(i = 1, 2)$ through the biasing current of CBTAs.

The coupling coefficient k for the proposed simulated transformer is found to be

$$k = \sqrt{\frac{M_{12}M_{21}}{L_pL_s}} = \frac{\sqrt{\dfrac{C_1R_3}{g_{m1}}\dfrac{C_2R_3}{g_{m2}}}}{\sqrt{\dfrac{(R_1 + R_3)C_1}{g_{m1}}\dfrac{(R_2 + R_3)C_2}{g_{m2}}}} = \frac{R_3}{\sqrt{(R_1 + R_3)(R_2 + R_3)}}\,. \tag{18}$$

5. Nonideal Analysis

Figure 6 shows the basic nonideal model of CBTA, including the essential nonidealities. The resistors and capacitors, besides representing the parasitic input and

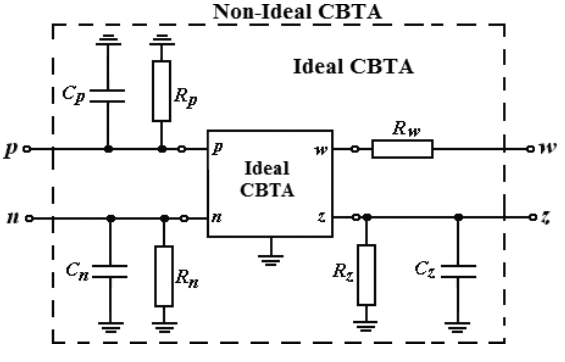


Fig. 6. The nonideal model of CBTA.

output impedances, also model the frequency dependency of the tracking gains of CBTA. R_p, R_n, R_z and R_w are the input and output resistances, respectively. C_p, C_n, C_z and C_w are the input and output capacitances, respectively. This approach is almost acceptable, provided that the implementations of the active devices do not employ multi-stage or complicated parts, which may insert additional poles or zeros to the frequency responses.

5.1. *Effect of tracking errors*

Taking into account the effects of the active component parameters in the circuit of Fig. 5(e), the two-port network matrix equations become

$$\begin{bmatrix} V_1(s) \\ V_2(s) \end{bmatrix} = \begin{bmatrix} s\dfrac{(R_1+R_3)C_1}{g_{m1}\mu_{w1}\alpha_{p1}} & s\dfrac{R_3C_1}{g_{m1}\mu_{w1}\alpha_{p2}} \\ s\dfrac{R_3C_2}{g_{m2}\mu_{w2}\alpha_{p1}} & s\dfrac{(R_2+R_3)C_2}{g_{m2}\mu_{w2}\alpha_{p2}} \end{bmatrix} \begin{bmatrix} I_1(s) \\ I_2(s) \end{bmatrix}. \tag{19}$$

Here, α_{pj} and μ_{wj} $(j = 1, 2)$ are the corresponding current and voltage nonideal gains, respectively, of the jth CBTA. Normalized active and passive sensitivities of L_1, L_2, M_{11}, M_{12}, M_{21}, and M_{22} are given by

$$S_{R_3}^{M_{11}} = S_{C_1}^{M_{11}} = S_{R_3}^{M_{12}} = S_{C_1}^{M_{12}} = S_{R_3}^{M_{21}} = S_{C_2}^{M_{21}} = S_{R_3}^{M_{22}} = S_{C_2}^{M_{22}} = 1\,, \tag{20a}$$

$$S_{g_{m1}}^{M_{11}} = S_{\mu_{w1}}^{M_{11}} = S_{\alpha_{p1}}^{M_{11}} = S_{g_{m1}}^{M_{12}} = S_{\mu_{w1}}^{M_{12}} = S_{\alpha_{p2}}^{M_{12}} = -1\,, \tag{20b}$$

$$S_{g_{m2}}^{M_{21}} = S_{\mu_{w2}}^{M_{21}} = S_{\alpha_{p1}}^{M_{21}} = S_{g_{m2}}^{M_{22}} = S_{\mu_{w2}}^{M_{22}} = S_{\alpha_{p2}}^{M_{22}} = -1\,, \tag{20c}$$

$$S_{R_1}^{L_1} = S_{C_1}^{L_1} = S_{R_2}^{L_2} = S_{C_2}^{L_2} = 1\,, \tag{20d}$$

$$S_{g_{m1}}^{L_1} = S_{\mu_{w1}}^{L_1} = S_{\alpha_{p1}}^{L_1} = S_{g_{m2}}^{L_2} = S_{\mu_{w2}}^{L_2} = S_{\alpha_{p2}}^{L_2} = -1\,. \tag{20e}$$

From Eqs. (20), normalized active and passive sensitivities of L_1, L_2, M_{11}, M_{12}, M_{21}, and M_{22} are no more than unity in magnitude. Thus, the proposed inductance offers low active and passive sensitivities. Such deviations can be overcome by using tuning via the bias current of CBTAs. Alternatively, the deviated inductances L_1, L_2, and M can be tolerated, by shifting the values of R_1, R_2, R_3, C_1, and C_2 from their nominal values, to achieve the desired oscillation frequency. It is also noted that the inductances L_1, L_2, and M of circuit deviations due to tracking errors are not more critical than the effect of absolute tolerances of the used resistors and capacitors (due to process tolerances, temperature effects, and aging).

5.2. *Effect of parasitic impedances*

Considering the above-mentioned nonidealities which are shown in Fig. 6, the passive components values of Fig. 5(e) including nonideal parasitic resistances and

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capacitances can be modified as follows:

$$Z'_{C1} = \frac{1}{sC_1}\left\|\frac{1}{sC_{z1}}\right\|R_{z1}, \quad Z'_{C2} = \frac{1}{sC_2}\left\|\frac{1}{sC_{z2}}\right\|R_{z2}\,, \tag{21a}$$

$$Z'_{R1} = R_1 + R_{w1}, \quad Z'_{R2} = R_2 + R_{w2}, \quad Z'_{R3} = R_3\,. \tag{21b}$$

The parasitic p and n terminal impedances can be modified as follows:

$$Z'_{p1} = \frac{1}{sC_{p1}}\left\|R_{p1}, \quad Z'_{p2} = \frac{1}{sC_{p2}}\right\|R_{p2}\,, \tag{22a}$$

$$Z'_{n1} = \frac{1}{sC_{n1}}\left\|R_{n1}, \quad Z'_{n2} = \frac{1}{sC_{n2}}\right\|R_{n2}\,. \tag{22b}$$

Therefore, the nonideal impedances L_1, L_2, M_{12}, and M_2 can be rewritten as

$$sL_p = \frac{(Z'_{R1} + Z'_{R3})}{g_{m1}\mu_{w1}\alpha_{p1}Z'_{C1}} = \frac{(R_1 + R_{w1} + R_3)}{g_{m1}\mu_{w1}\alpha_{p1}\left(\dfrac{1}{sC_1}\left\|\dfrac{1}{sC_{z1}}\right\|R_{z1}\right)}\,, \tag{23a}$$

$$sL_s = \frac{(Z'_{R2} + Z'_{R3})}{g_{m2}\mu_{w2}\alpha_{p2}Z'_{C2}} = \frac{(R_2 + R_{w2} + R_3)}{g_{m2}\mu_{w2}\alpha_{p2}\left(\dfrac{1}{sC_2}\left\|\dfrac{1}{sC_{z2}}\right\|R_{z2}\right)}\,, \tag{23b}$$

$$sM_{12} = \frac{Z'_{R3}}{g_{m1}\mu_{w1}\alpha_{p2}Z'_{C1}} = \frac{R_3}{g_{m1}\mu_{w1}\alpha_{p2}\left(\dfrac{1}{sC_1}\left\|\dfrac{1}{sC_{z1}}\right\|R_{z1}\right)}\,, \tag{23c}$$

$$sM_{21} = \frac{Z'_{R3}Z'_{C2}}{g_{m2}\mu_{w2}\alpha_{p1}} = \frac{R_3}{g_{m2}\mu_{w2}\alpha_{p2}\left(\dfrac{1}{sC_2}\left\|\dfrac{1}{sC_{z2}}\right\|R_{z2}\right)}\,. \tag{23d}$$

The nonideal coupling coefficient k including parasitic impedances for the proposed simulated transformer can be rewritten as

$$k = \sqrt{\frac{M_{12}M_{21}}{L_pL_s}} = \frac{\sqrt{\dfrac{Z'_{R3}}{g_{m1}Z'_{C1}s}\,\dfrac{Z'_{R3}}{g_{m2}Z'_{C2}s}}}{\sqrt{\dfrac{(Z'_{R1} + Z'_{R3})}{g_{m1}Z'_{C1}s}\,\dfrac{(Z'_{R2} + Z'_{R3})}{g_{m2}Z'_{C2}s}}}$$

$$= \frac{Z'_{R3}}{\sqrt{(Z'_{R1} + Z'_{R3})(Z'_{R2} + Z'_{R3})}} = \frac{R_3}{\sqrt{(R_1 + R_{w1} + R_3)(R_2 + R_{w2} + R_3)}}\,. \tag{24}$$

From Eqs. (21a)–(24) it can be seen that the parasitic components of CBTAs affect the performance of the proposed circuit. However, the parasitic resistors R_{w1} and R_{w2} can be tolerated by choosing the external resistor values large enough. Also, by selecting the external capacitor values large enough with respect to the terminal

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capacitances, the latter can be ignored. In fact:

(i) For the first CBTA, the total impedance at the terminal z is $\frac{1}{\omega C_1}||\frac{1}{\omega C_{z1}}||R_{z1}$. When the impedance $\frac{1}{\omega C_1}$ is chosen much smaller than $\frac{1}{\omega C_{z1}}$ and R_{z1} then the equivalent impedance is nearly equal to $\frac{1}{\omega C_1}$.

(ii) For the second CBTA, the total impedance at the terminal z can be written as $\frac{1}{\omega C_2}||\frac{1}{\omega C_{z2}}||R_{z2}$. Similarly, when the impedance $\frac{1}{\omega C_2}$ is chosen much smaller than $\frac{1}{\omega C_{z2}}$ and R_{z2}, then the equivalent impedance is nearly equal to $\frac{1}{\omega C_2}$.

(iii) For the first CBTA, the total parasitic impedance at the terminal w is $R_1 + R_{w1}$. If R_1 is chosen much larger than R_{w1}, then the equivalent impedance is nearly equal to R_1.

(iv) For the second CBTA, the total parasitic impedance at the terminal w is $R_2 + R_{w2}$. If R_2 is chosen much larger than R_{w1}, then the total impedance is nearly equal to R_2.

6. Simulation Results

The characteristics of the proposed circuits have been verified using PSPICE simulations. The CBTAs are simulated using the schematic implementation shown in Fig. 2, with DC power supply voltages equal to $V_{DD} = -V_{SS} = 1.5\,\text{V}$. The simulations are performed using $0.18\,\mu$m level-7 TSMC CMOS technology parameters.

The proposed synthetic transformer circuit of Fig. 5 was used to simulate the circuit shown in Fig. 7 with $C_p = C_s = 100\,\text{pF}$ and $R_p = R_s = 10\,\text{k}\Omega$. The synthetic transformer circuit of Fig. 5(e) is built with $R_1 = R_2 = 500\,\Omega$, $R_3 = 250\,\Omega$, $g_m = 0.5\,\text{mS}$, and $C_1 = C_2 = 200\,\text{pF}$ to obtain $M_{11} = M_{12} = M_{21} = M_{22} = 100\,\mu\text{H}$, $L_1 = L_2 = 200\,\mu\text{H}$, and $L_p = L_s = 300\,\mu\text{H}$ and resulting in $f_o = 918.88\,\text{kHz}$ and the quality factor $Q = 5.77$. By using these parameters, k can be calculated as 0.33. Note that the g_m value of CBTA is found by taking the bias current $I_B = 100\,\mu\text{A}$.

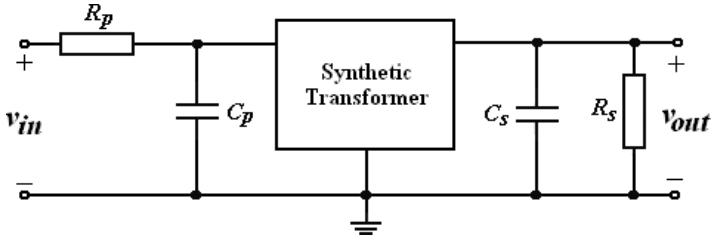


Fig. 7. Band-pass filter example using presented synthetic transformer.[8]

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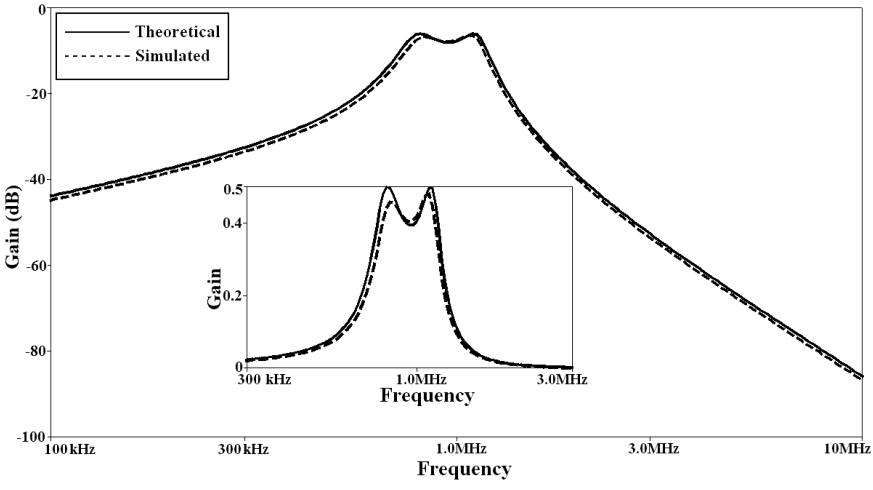


Fig. 8. Gain characteristics of the theoretical and simulated band-pass filters in Fig. 7.

The magnitude and the phase characteristics of the filter are shown in Figs. 8 and 9, respectively. It appears from Figs. 8 and 9 that the theoretical and simulated results are in good agreement.

To test the electronically tunability of L_1, L_2, and M of the proposed transformer with bias currents, the results shown in Fig. 10 are presented. In these simulations, the bias currents I_B are chosen as 50, 100, and 150 μA, respectively, while keeping the passive component values as the same. Therefore, the transconductance gains are obtained as 0.34, 0.5, and 0.61 mS, respectively.

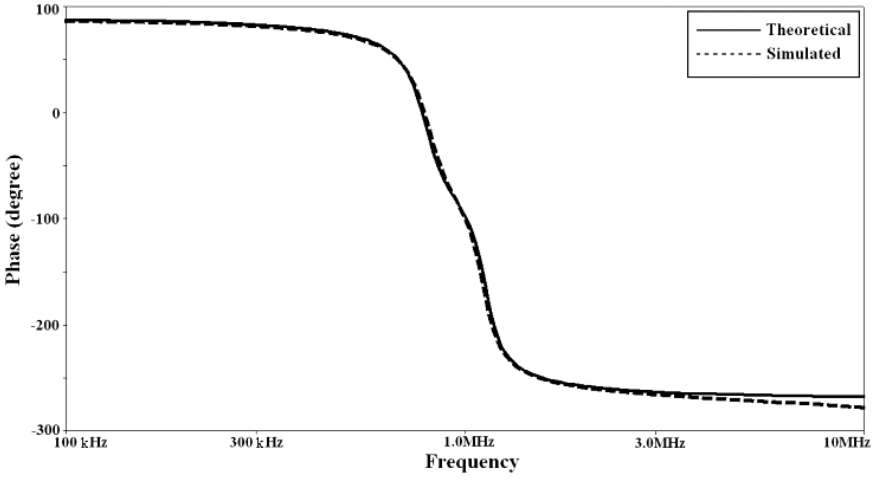


Fig. 9. Phase characteristics of the theoretical and simulated band-pass filters in Fig. 7.

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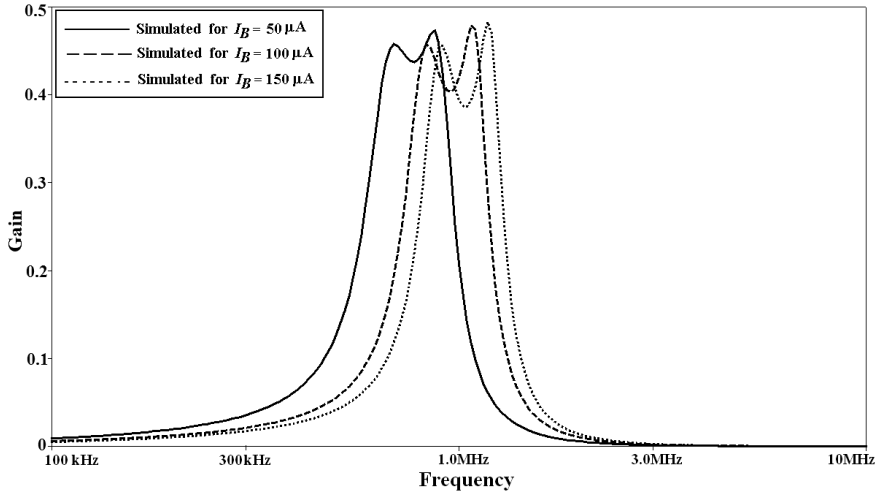


Fig. 10. Tuning of L_1, L_2, and M of the proposed transformer.

The performance of the proposed synthetic transformer is compared with the one reported in the literature[8] by employing them in the band-pass filter example of Fig. 7. For these simulations, the passive component values are chosen as $C_p = C_s = 100\,\text{nF}$, $R_p = R_s = 10\,\text{k}\Omega$, $R_1 = R_2 = 1\,\text{k}\Omega$, $R_3 = 500\,\Omega$, $g_m = 0.5\,\text{mS}$, and $C_1 = C_2 = 100\,\text{nF}$ to obtain $L_p = L_s = 0.3\,\text{H}$ and $M_{11} = M_{12} = M_{21} = M_{22} = 0.1\,\text{H}$, resulting in $f_o = 918.88\,\text{Hz}$ and the quality factor $Q = 5.77$. The simulation results can be seen in Fig. 11. From Fig. 11, the errors are within the expected limits and they are originating from the nonidealities of CBTAs.

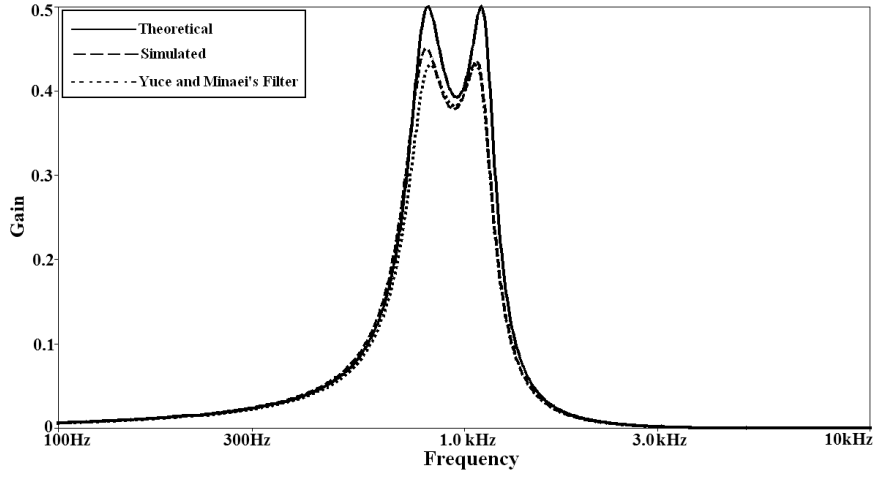


Fig. 11. Band-pass responses comparison of the filters in Fig. 7 and the ones reported in the literature.[8]

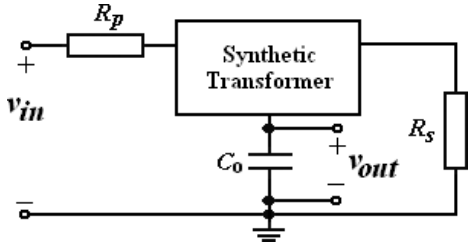


Fig. 12. Low-pass filter example to test the presented floating synthetic transformer.

In order to demonstrate the floating property of the proposed transformer, the low-pass filter shown in Fig. 12 is set up. For these simulations, the passive component values are chosen as $R_p = R_s = 1\text{k}\Omega$, $C_0 = 100\,\text{pF}$, $L_p = L_s = 20\,\mu\text{H}$, and $M_{11} = M_{12} = M_{21} = M_{22} = 10\,\mu\text{H}$ resulting in corner frequency of $f_o = 4.5\,\text{MHz}$. $R_1 = R_2 = 500\,\Omega$, $R_3 = 500\,\Omega$, $g_m = 0.5\,\text{mS}$, and $C_1 = C_2 = 10\,\text{pF}$ are chosen for the circuit of Fig. 5(e) to obtain the above-mentioned L_p, L_s, and M values. The simulation results with respect to theoretical ones can be shown in Fig. 13. It can be seen from Fig. 13 that the magnitudes of the simulated and theoretical responses of the filter are in good agreement.

Due to the nonidealities of CBTA, some discrepancies are exhibited between the theoretical and simulation results as shown in Figs. 8–10 and 12. In order to find the maximum operating point and nonidealities of CBTA, the PSPICE simulations are also done by using the above-mentioned transistor model. Therefore, corner frequencies are found as $\omega_{\alpha p} = 1100\,\text{Mrad/s}$, $\omega_{\alpha n} = 960\,\text{Mrad/s}$, $\omega_{gm} = 1100\,\text{Mrad/s}$, and $\omega_{\mu} = 9430\,\text{Mrad/s}$, and errors of these gains are $\varepsilon_{\alpha p} = -0.0032$, $\varepsilon_{\alpha n} = 0.001$,

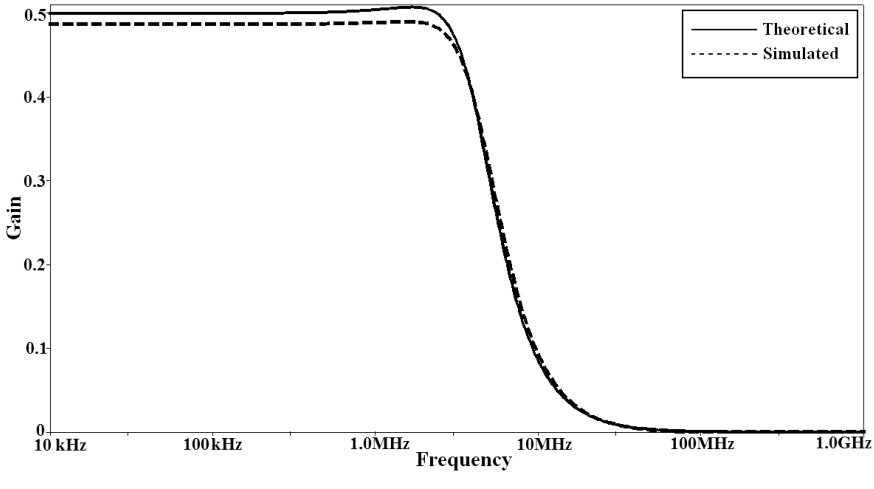


Fig. 13. Simulation results for floating implementation.

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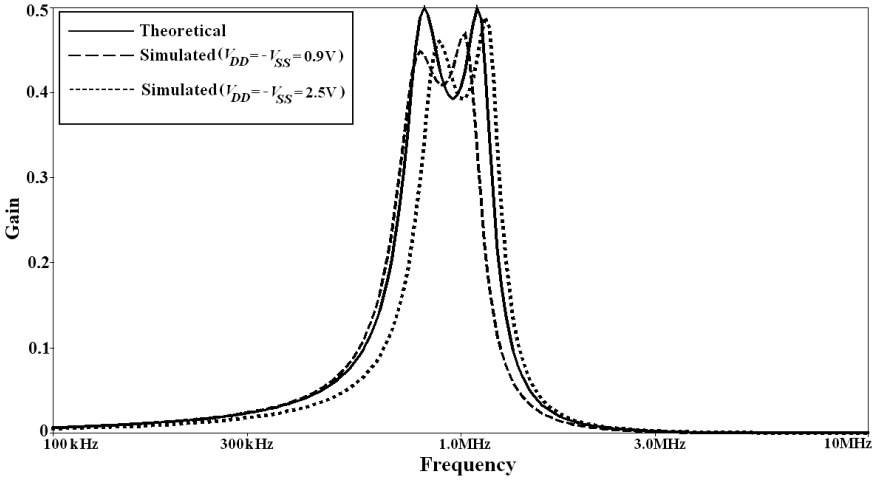
Table 3. Parasitic impedances of CBTA.

Parasitic impedances	Values
R_p	74 kΩ
R_n	69 kΩ
R_z	377 kΩ
R_w	130 Ω
C_p	300 fF
C_n	620 fF
C_z	150 fF

$\varepsilon_{gm} = 0.04$, and $\varepsilon_{\mu} = 0.089$. As a result, the maximum operating frequency of CBTA can be found as follows $f_{\max} = \min\{f_{\alpha p}, f_{\alpha n}, f_{gm}, f_{\mu}\} \approx 150\,\text{MHz}$.

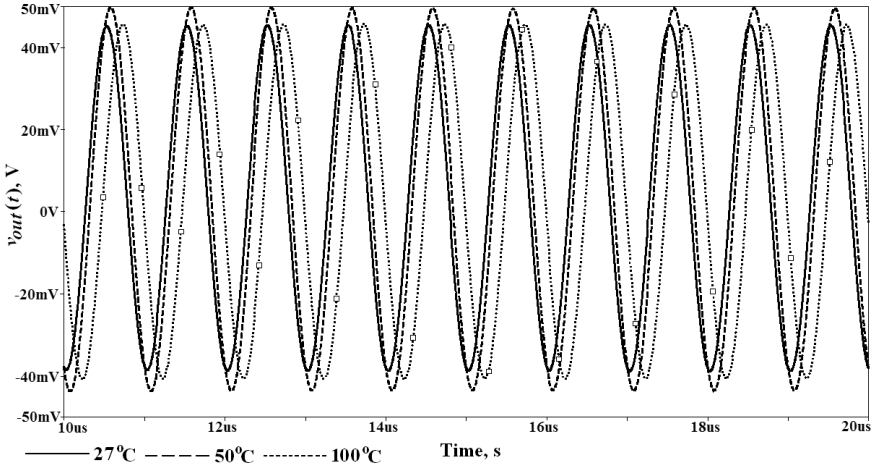
The CBTA has parasitic resistances and capacitances as shown in Fig. 6. The parasitic resistances and capacitances of CBTA are given in Table 3. These parasitic capacitances and resistances are obtained from the CMOS structure of CBTA through AC simulations and are adopted with the equivalent circuit shown in Fig. 6.

The simulations are also done by using various values of the DC power supply voltages. The simulation results for $V_{DD} = -V_{SS} = 0.9\,\text{V}$ and $V_{DD} = -V_{SS} = 2.5\,\text{V}$ supply voltages are give in Fig. 14(a). It can be seen from Fig. 14(a) that the magnitudes of the theoretical and simulated responses of the proposed transformer are in good agreement. In addition, the output voltage versus temperature variation is



(a)

Fig. 14. (a) The simulation results for various values of the DC power supply voltages and (b) the simulation results for the output voltage versus temperature variations.



(b)

Fig. 14. (*Continued*)

given in Fig. 14(b). For these simulations, the input signal is taken as a sinusoidal signal with 0.1 V peak value and 1 MHz frequency and the simulations are done under different temperatures. The total power dissipation of the proposed circuit is about 3.8 mW.

7. Experimental Results

In order to demonstrate the workability of the proposed synthetic transformer circuit, the band-pass filter is constructed using commercially available active devices, namely AD844s, and LM13700.[35,36] The CBTA is realized using three AD844s and one LM13700 as shown in Fig. 15. Since the IC of CBTA is not available at present,

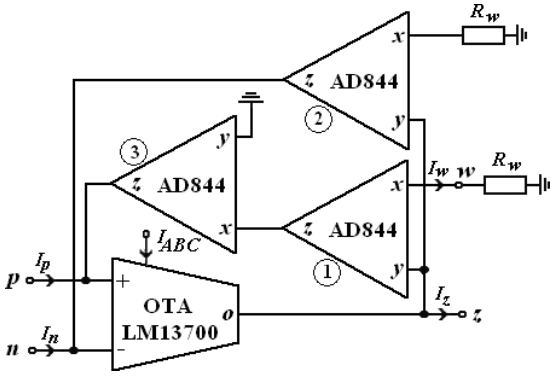


Fig. 15. Implementation of CBTA using the commercially available active devices.

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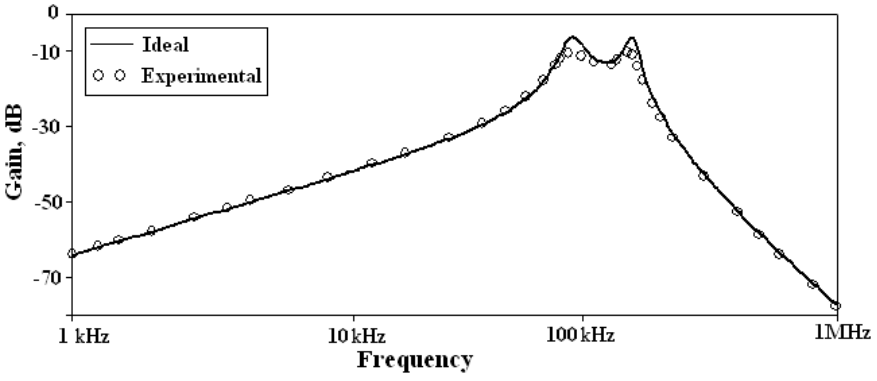


Fig. 16. Ideal and experimental results of the band-pass filter in Fig. 7.

to show the workability of the proposed configuration it is tested with commercially available elements such as AD844s.

Commercially available LM13700 is used for the transconductance section of CBTA. The g_m value of LM13700 is adjusted by the I_{ABC} current,[36] where I_{ABC} is the amplifier bias current of LM13700 and it is adjusted to set $g_m = 10\,\text{mS}$ for all the experiments. It is important to note that, in order for the implementation of CBTA to work properly in Fig. 15, R_w resistors in Fig. 15 should be chosen to be equal. The performance of the filter topology given in Fig. 7 is verified using experimental study. The passive components are chosen as $C_p = C_s = 1\,\text{nF}$, $R_p = R_s = 10\,\text{k}\Omega$, $C_1 = C_2 = 1\,\text{nF}$, and $R_1 = R_2 = R_3 = 10\,\text{k}\Omega$, resulting in $M_{11} = M_{12} = M_{21} = M_{22} = M = 1\,\text{mH}$, $L_1 = L_2 = 1\,\text{mH}$, $L_p = L_s = 2\,\text{mH}$, $k = 0.5$, $f_o = 112.54\,\text{kHz}$, and $Q = 7.07$. The comparison of experimental results with the theoretical ones can be seen in Fig. 16.

8. Conclusions

In this work, the modified Gorski-Popiel technique and a new synthetic floating transformer circuit are presented. The proposed synthetic floating transformer circuit uses two CBTAs, three resistors, and two grounded capacitors which are more suitable for IC fabrication. The primary self-inductance, the secondary self-inductance, and the mutual inductance can be independently controlled and can be tuned electronically by changing the biasing current of CBTA. It has a good sensitivity performance with respect to circuit and CBTA parameters. The workability of the proposed circuits is demonstrated by both PSPICE simulations and experimental results.

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